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# FAULT TOLERANT PARALLEL FILTERS BASED ON ERROR CORRECTION CODES

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## ABSTRACT

Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters' structure and properties to achieve fault tolerance have been proposed. A new scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost.

***Keywords*:** Air pollution, wireless sensor system, carbon monoxide, smoke, PHP-MYSQL, LabVIEW

## 1. INTRODUCTION

The Digital Filters plays a vital role in the analog and digital communication. The main purpose of using the filters is to eliminate the undesired signal components thereby providing the better quality signal at the output. The digital filters having the unique characteristics of

generating the stabilized signal at the output while compared with the analog filters. So that the digital filters are more preferable than the analog one. There are two main kinds of digital filters they are 1.FIR (Finite Impulse Response) and 2.IIR (Infinite Impulse Response) filter. The FIR filter is preferred over the IIR filter because of efficient hardware implementation with fewer precision errors and also giving the stabilized response with the linear phase [1],also helps to know more about parallel processing. The Pipelining as well as the Parallel Processing techniques can reduce the power consumption by lowering the supply voltage when the sampling speed does not increase.

In order to reduce the large amount of hardware cost a new technique is being proposed called as the Iterated Short Convolution Algorithm (ISC) [2].This ISC based technique is being transposed to get the hardware efficient FIR Filter structure. This technique is highly effective when the length of the FIR filter is large. This method is based on the mixed radix algorithm and the fast convolution algorithm. The application of Error Correction Code is being briefly studied using [3].One beneficial method that the exchange of adders with the multipliers because the adders which are weighing less as compared with the multipliers in case of silicon area [4].This proposed filter structure exploits the symmetric filter coefficients thereby reducing the number of multipliers in the sub filter section with the expense of increasing the additional adders in the pre-processing and post processing blocks.

## 2. EXISTING METHOD

Some memory protection architectures based on nonlinear codes also have been proposed in the community. In efficient single error correcting and d(d _ 2)-unidirectional error detecting codes were used to protect memories. Another nonlinear error detecting code – Berger code, was used to detect unidirectional errors in flash memories. These existing protection architectures based on nonlinear codes, however, were mainly designed for unidirectional error models. In the presence of symmetric errors, the reliability of the protected memory systems can not be guaranteed. Nonlinear robust codes have been proposed as a solution to the limitation of minimum distance linear error detecting codes in the presence of multi-bit errors. The nonlinear robust codes are designed to provide equal protection against all errors thereby eliminating possible weak areas in the protection. Several variants of robust codes have been proposed. These variants allow tradeoffs in terms of robustness and hardware overhead for many architectures.

## 3. PROPOSED METHOD

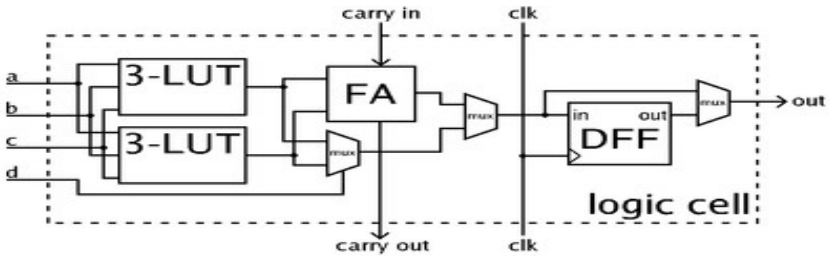


**Figure 1 System Hardware**

In general, a logic block (CLB or LAB) consists of a few logical cells (called ALM, LE, Slice etc). A typical cell consists of a 4-input Lookup table (LUT), a Full adder (FA) and a D-type flip-flop, as shown below. The LUT are in this figure split into two 3-input LUTs. In normal mode those are combined into a 4-input LUT through the left mux. In arithmetic mode, their outputs are fed to the FA. The selection of mode are programmed into the middle mux. The output can be either synchronous or asynchronous, depending on the programming of the mux to the right, in the figure example. In practice, entire or parts of the FA are put as functions into the LUTs in order to save space.

## 4. SYSTEM IMPLEMENTATION AND THE RESULTS

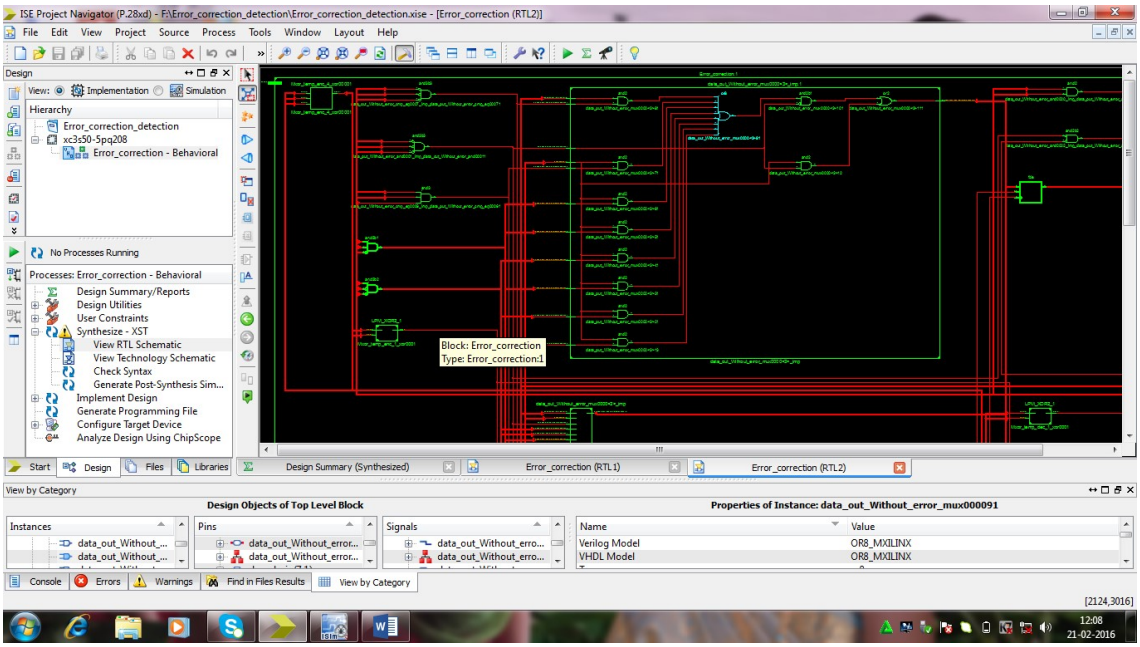


**Figure 2 Error Correction Architecture Diagram**

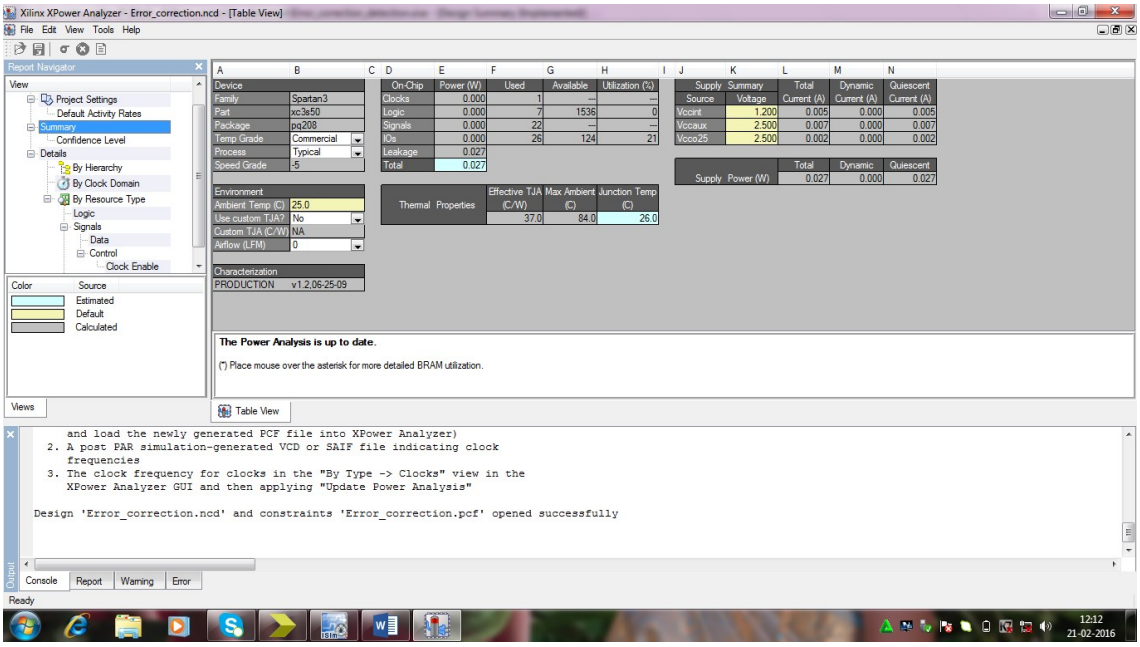


**Figure 3 Error Correction and Detection**

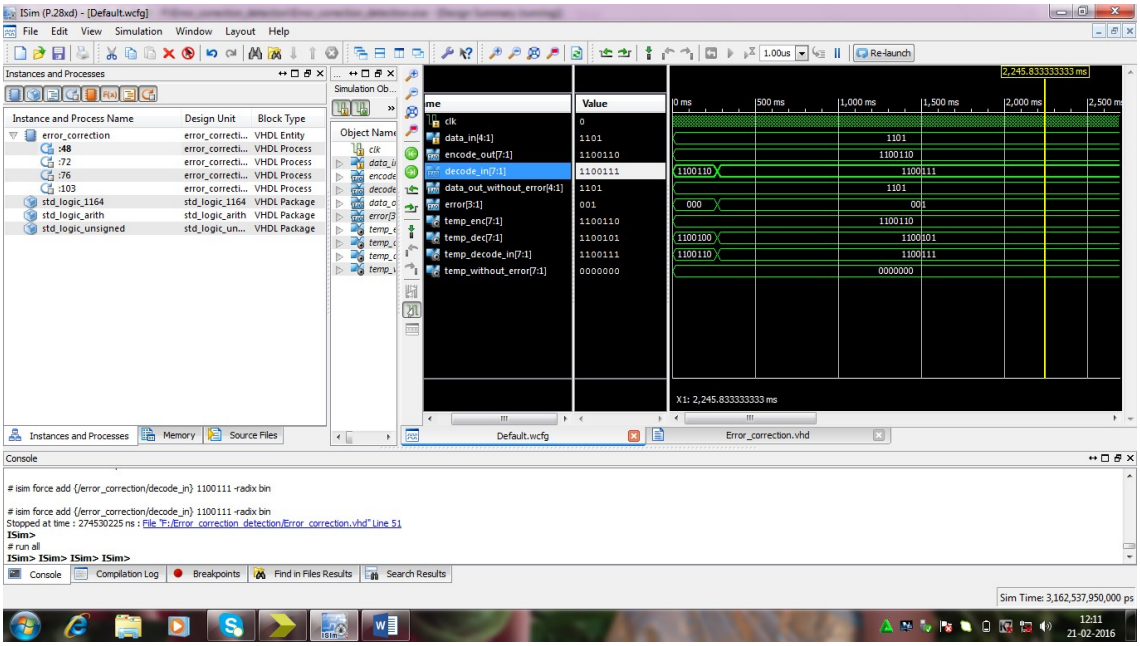


**Figure 4 Power Result**

The values of the level of smoke and temperature from the serial port is taken in account by the LabVIEW software which is used to display these data in their respective textbox and

also it displayed in the form of continuous waveforms in two different panel. The screenshot of the computer window for the LabVIEW designed page is shown below.

## 5. CONCLUSION

We have presented a scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The proposed scheme can also be applied to the FIR filters The technique is evaluated using a only two redundant filter to achieve the high error correction in ECC which also reduces the area, delay and power than previous. This will be of interest when the number of parallel filters is small as the cost of the proposed scheme is larger in that case.

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