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Heterogate junctionless tunnel field-effect transistor: future of low-power devices

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Abstract Gate dielectric materials play a key role in device development and study for various applications. We illustrate herein the impact of hetero (high-k/low-k) gate dielectric materials on the ON-current (I_{ON}) and OFF-current (I_{OFF}) of the heterogate junctionless tunnel field-effect transistor (FET). The heterogate concept enables a wide range of gate materials for device study. This concept is derived from the well-known continuity of the displacement vector at the interface between low- and high-k gate dielectric materials. Application of high-k gate dielectric material improves the internal electric field in the device, resulting in lower tunneling width with high I_{ON} and low I_{OFF} current. The impact of work function variations and doping on device performance is also comprehensively investigated.

Keywords Heterogate · JLTFET · Displacement vector · High-k · Low-k · Tunneling width · MOSFET · Gate work function

1 Introduction

Aggressive scaling of bulk metal–oxide–semiconductor (MOS) FETs has played a significant role in the continuous development of ultrascaled highly dense complementary MOS (CMOS) circuits for more than three decades. As conventional bulk MOSFETs are scaled down below 45 nm, short-channel effects (SCEs) and subthreshold leakage currents become more problematic [1]. The OFF-state leakage current (I_{OFF}) is mainly responsible for the subthreshold power dissipation ($I_{OFF} \cdot V_{DD}$) in very large-scale integration (VLSI) circuits. Due to their nonscalable subthreshold slope (SS) behavior at 300 K, MOSFETs fail to fulfill present requirements for low-power applications. Nowadays, a promising candidate to replace the conventional FET structure is the tunnel FET (TFET), which has become very attractive for use in ultralow-power applications due to its low OFF-current (I_{OFF}) and stepper subthreshold slope (SS) (<60 mV/decade) [2–6].

However, the tunneling FET structure suffers from lower ON-current than conventional MOSFETs due to tunneling current transport phenomena. To overcome this challenge of low ON-current (I_{ON}), various approaches have been used to improve the electric field inside the tunneling region and reducing the effective tunneling bandgap [7–13]. However, lowering the bandgap increases I_{OFF} and limits the power supply scaling V_{DD} according to $E_G \geq q V_{DD}$ [14–17].

At lower technology nodes, the requirement for shallow junctions is fulfilled by using the junctionless architecture proposed by Colinge [18–21], which is the focus of this work. Junctionless devices having no p–n junctions show improved device performance compared with conventional architectures based on p–n junctions. In this study, the advantages of the junctionless transistor are captured by adopting the junctionless TFET (JLTFET) structure. To improve the ON-current (I_{ON}) and suppress the OFF-current (I_{OFF}) as well as the subthreshold slope (SS), a broken-bandgap source/channel AlGaAs/Si semiconductor is used [18–26]. The remainder of this paper is arranged as follows:

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Sect. 2 describes the simulation setup and device operation. Results and discussion are summarized in Sect. 3. Finally, concluding remarks are provided in Sect. 5.

2 Simulation setup

A schematic of the heterogate JLTFET considered in this work is shown in Fig. 1. The device structure is derived from a conventional *p*–i–*n* diode. The device has uniformly doped 5-nm-thick AlGaAs/Si with oxide thickness of 2 nm. Both the control gate length (L_G) and auxiliary gate length (L_{G1}) are 20 nm.

The transport phenomena in tunneling devices are completely different from those occurring in bulk MOSFET devices. Current conduction in the TFET is governed by band-to-band (B2B) tunneling from valence band of source to conduction band of channel [1–5]. Such B2B tunneling is much more sensitive to material/device parameters such as energy bandgap (E_G), dielectric thickness (t_{ox}), dielectric constant of the gate material (k), and effective mass of charge carriers (m^*), according to Eq. 1 [1,5,7,10]:

$$T(E) = \exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3|e|\hbar(\Delta\Phi + E_G)}\lambda\right), \quad (1)$$

where λ is the tunneling distance between source and channel, given by

$$\lambda = \sqrt{(\varepsilon_{Si}/\varepsilon_{ox})\, t_{ox} t_{Si}}.$$

In Eq. 1, m^* is the effective mass , $\Delta\Phi$ is the band energy difference between conduction band of source and valence band of channel, $\hbar$ and q are the reduced Planck constant and electron charge, respectively, while t_{ox} and t_{Si} are the physical oxide thickness and semiconductor channel thickness, respectively.

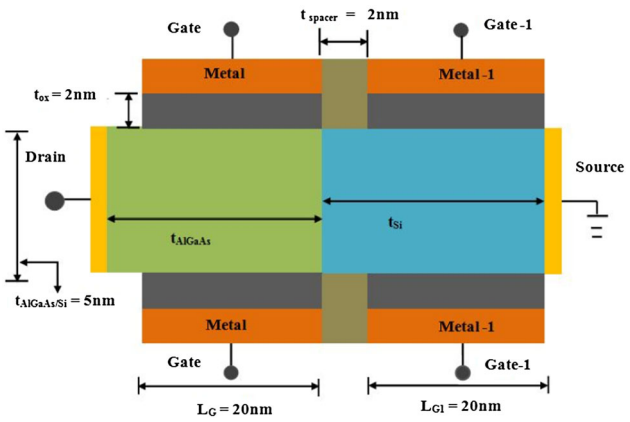

Fig. 1 Device structure and parameters of the heterogate junctionless TFET

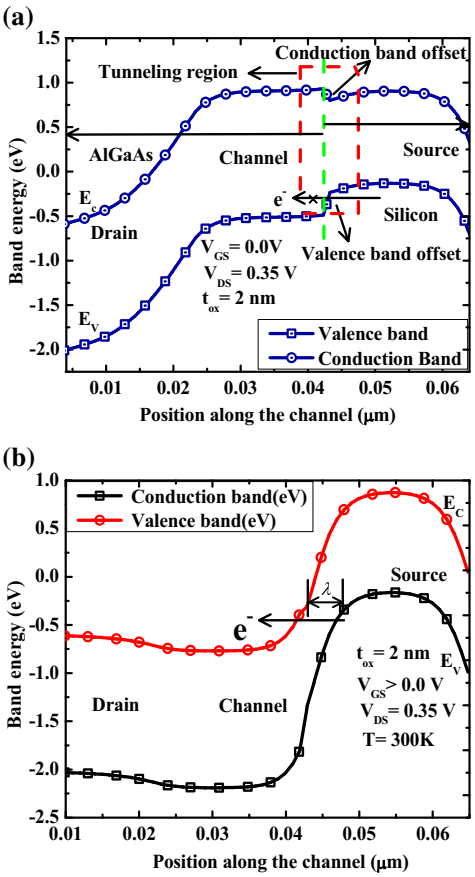

Fig. 2 Simulated band structure of the heterogate JLTFET: **a** OFF-state ($V_{GS} = 0.0$ V) and **b** ON-state ($V_{GS} = 1.0$ V) at $V_{DS} = 0.35$ V for high-k gate material HfO_2 ($k = 25$)

In this work, simulations were carried out using Silvaco Atlas [23,25,26]. In the simulations, a nonlocal model was considered for band-to-band tunneling of charge carriers between source and channel. Due to the high doping level, a source bandgap narrowing (BGN) model was also included, because the effective bandgap directly influences the tunneling current. We included a Shockley–Read–Hall (SRH) recombination model due to the presence of high impurity atom concentration in the channel and Fermi–Dirac statistics to calculate the intrinsic carrier concentration. For more accurate current calculations, Schenk's trap-assisted tunneling (TAT), drift–diffusion current transport model, and quantum confinement (QC) models were also included [23,27,28].

The simulated energy-band diagram for OFF-state ($V_{GS} = 0.0$ V) and ON-state ($V_{GS} = 1.0$ V) are shown in Fig. 2. Figure 2a shows the OFF-state behavior of the device, revealing that the tunneling width (λ) is larger as a result of the small leakage current. In the ON-state condition (Fig. 2b), the tunneling width (λ) reduces as a result of the increased tunneling

probability of charge carriers from valence band of source to conduction band of channel.

3 Results and discussion

Tunnel FETs suffer from low ON-current (I_{ON}) due to the B2B tunneling mechanism. The tunneling current largely depends on the tunneling distance (λ). Minor changes in device parameters such as the bandgap (E_g), oxide gate material, etc. can improve the ON-current (I_{ON}) [29–31], as discussed in Sect. 2, and the TFET characteristics are even more sensitive to the oxide thickness (t_{ox}), doping profile, and dielectric constant of the gate material (k). In this section, the effect of high-k dielectric, gate work function, and source/channel/drain doping profile on device characteristics is presented based on simulation results and discussed in detail.

3.1 Impact of high-k gate materials

Figure 3a compares the electric field profile inside a heterogate JLTFET. Conventionally, the electric field in this device is given by Eq. (2), where S is the separation between the high-k and low-k material.

$$\xi \approx \frac{V_1 - V_2}{S}. \tag{2}$$

As shown in Fig. 3b, c, when using a high-k dielectric in the heterogate JLTFET, at the interface between the dielectrics, the displacement vector ($D = \varepsilon\xi$) should be continuous [8]:

$$\varepsilon_1\xi_1 = \varepsilon_2\xi_2, \tag{3}$$

$$\xi_2 = \left(\frac{\varepsilon_1}{\varepsilon_2}\right)\xi_1. \tag{4}$$

At the interface between the high-k and low-k dielectric, one has

$$\varepsilon_1 \gg \varepsilon_2 \tag{5}$$

$$\xi_2 > \xi_1; \tag{6}$$

i.e. the electric field is larger toward the low-k dielectric, strongly supporting the asymmetric electric field behavior of TFET devices as shown in Fig. 3a. The physical interpretation of the displacement vector in a heterogate JLTFET is shown in Fig. 3b. Application of a high-k gate material in a heterogate JLTFET increases the electric field lines from the source side and reduces the barrier width near the source–channel interface. The electric field variation along the channel in a heterogate JLTFET with different gate dielectric materials

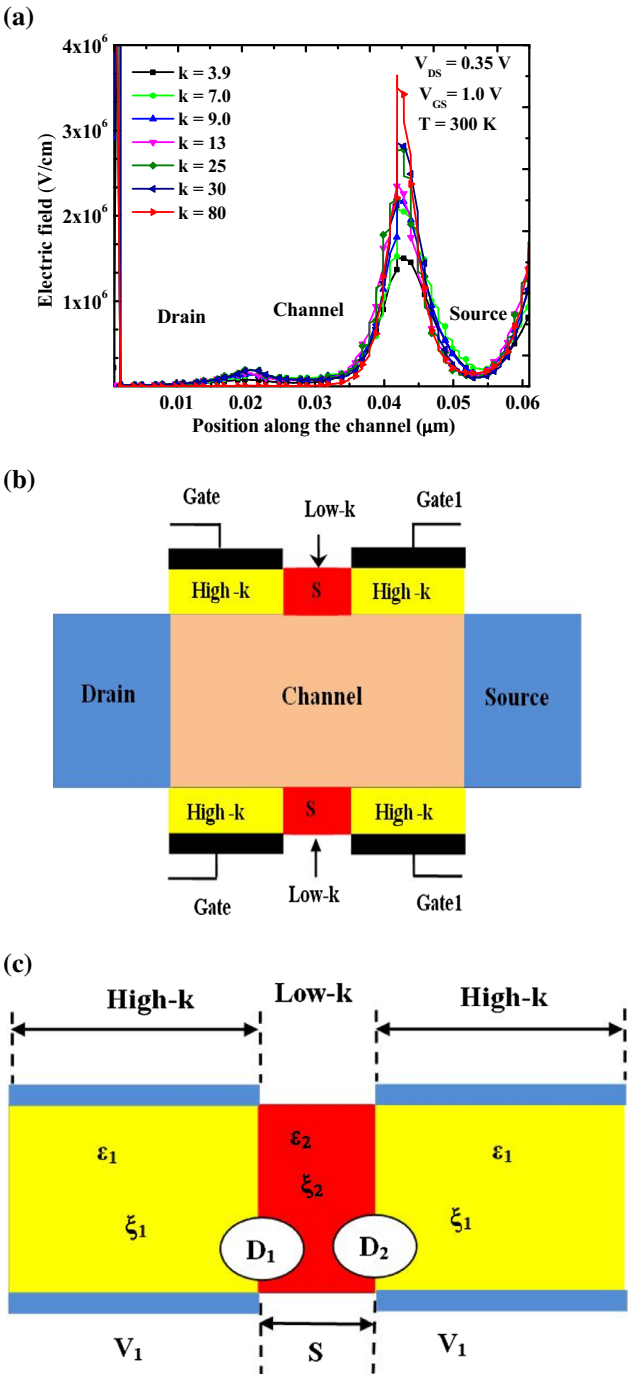

Fig. 3 **a** Electric field distribution along the channel for various gate dielectric materials in the ON-state. **b** Physical interpretation of displacement vector in the heterogate JLTFET. **c** Illustration of the electric field amplification using low-k/high-k dielectrics in the heterogate JLTFET

is shown in Fig. 3a. As the k value of the gate material is varied from low to high, the electric field increases and the peak electric field shifts towards the source end. Due to this increased electric field, the conduction as well as valence

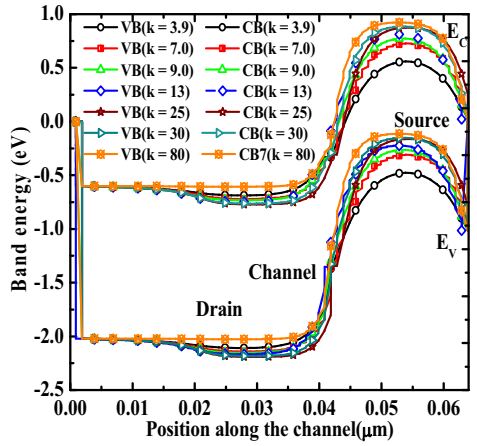

Fig. 4 Band shift versus gate dielectric material in the ON-state

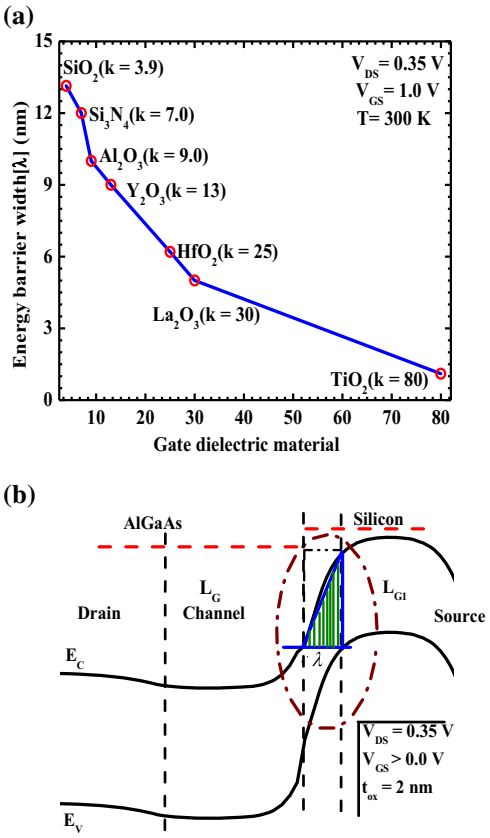

Fig. 5 **a** Tunneling barrier width (λ) modulation versus various gate dielectric materials for $t_{ox} = 2$ nm, $N_d = 1 \times 10^{19}/cm^3$, and spacer = 2 nm for SiO_2 ($k = 3.9$). **b** Measurement procedure for tunneling barrier width (λ) of **a**, using the WKB triangular potential approximation

band move upwards, as shown in Fig. 4. This upward shift of the bands reduces the tunneling barrier (λ).

As per Eq. 1, the quantum-mechanical tunneling probability is an exponential function of barrier width (λ). Figure 5a shows the variation of the energy barrier width (λ) reduction versus the gate dielectric material for the simulated device.

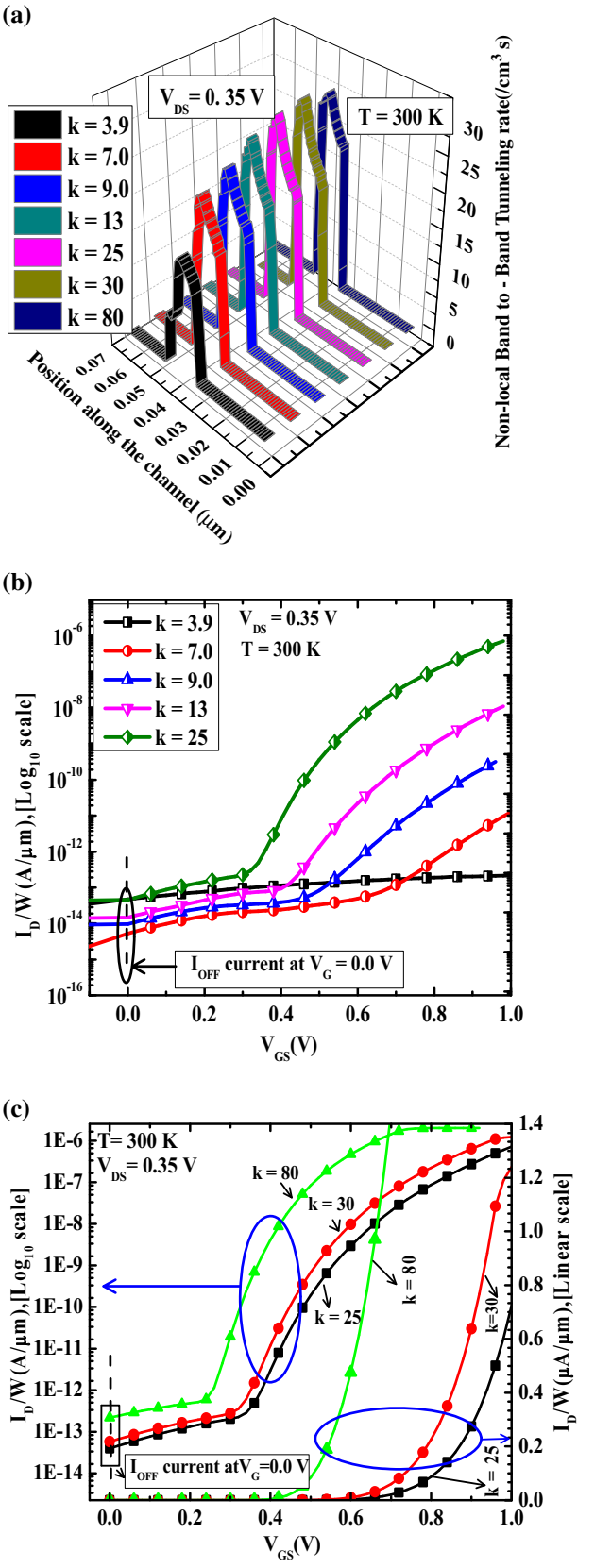

Fig. 6 Impact of high-k gate dielectric on **a** nonlocal band-to-band (B2B) tunneling rate, **b** and **c** I_D–V_G characteristics for drain voltage $V_{DS} = 0.35$ V

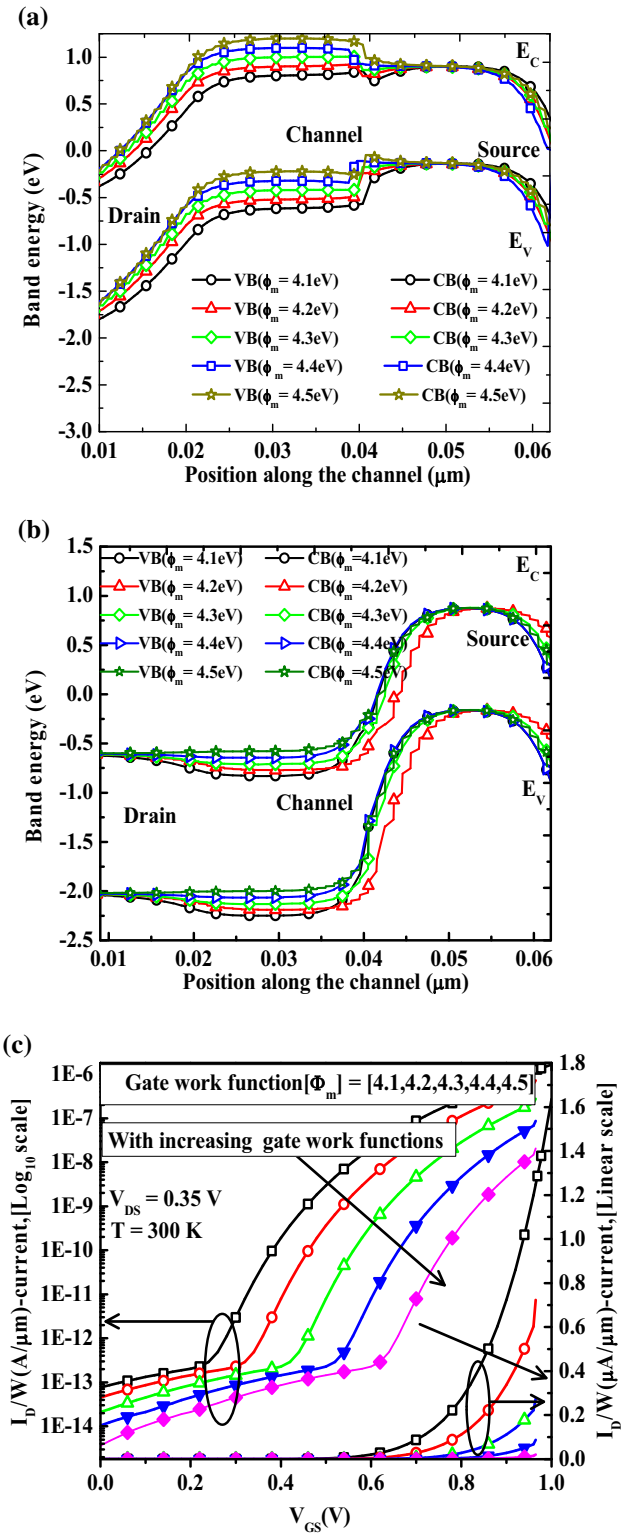

Fig. 7 Effect of control gate work function on the band diagram in **a** the OFF-state and **b** the ON-state, and **c** the I_D–V_G characteristic

The simulation results strongly support the variation behavior of the tunneling distance with the gate dielectric material [9]. Figure 5b shows a graphical representation of the technique used for measurement of the tunneling barrier width

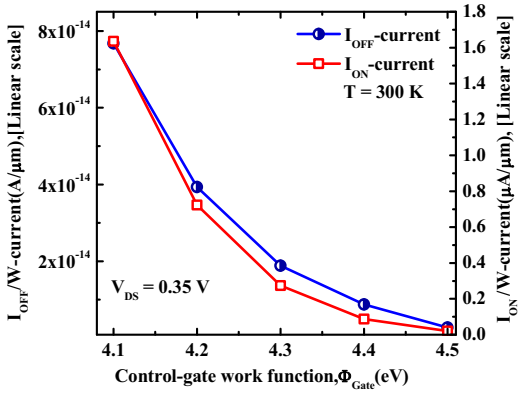

Fig. 8 I_{ON}, I_{OFF} current variation for the considered device when varying the control gate work function with $N_d = 1\times10^{19}/\text{cm}^3$, $t_{ox} = 2\,\text{nm}$, spacer = 5 nm, and $\Phi_{m1} = 5.2\,\text{eV}$

(λ), adopting the Wentzel–Kramers–Brillouin (WKB) triangular potential approximation [11].

The reduction of the tunneling barrier width (λ) when employing a high-k gate dielectric material results in high electric field that improves the Zener tunneling rate of electrons from valence band (E_V) of source to conduction band of channel. The simulated nonlocal B2B tunneling rate versus the high-k gate material for the heterogate JLTFET device is shown in Fig. 6, revealing improved nonlocal tunneling in the device. The tunneling rate extracted for the simulated device varies from 5.0 to 27.5/cm^3 s for the various gate dielectric materials with $k = 3.9 - 80$, as shown in Fig. 6a. The ON-current (I_{ON}) is proportional to the electron tunneling rate, which according to Eq. 1 is dependent on the tunneling barrier width (λ). Therefore, the reduction in the tunneling barrier width (λ) when using a high-k dielectric gate material will increase the drain current as compared with low-k dielectric material.

In TFETs, the ON-current (I_{ON}) is proportional to the electron tunneling rate, which follows the transmission probability T_{WKB} according to Eq. (1). The effect of high-k gate material on the I_D–V_G characteristic of the heterogate JLTFET device is shown in Fig. 6b, c. The high-k gate material increases the capacitive coupling, resulting in a major improvement in I_{ON} as well as the average subthreshold swing (SS) [8]. Based on the WKB tunneling probability in Eq. (1), the tunneling current increases when increasing the electric field along the channel, as shown in Fig. 3a. One way of increasing the electric field is by decreasing the oxide thickness (t_{ox}). However, a critical decrease in oxide thickness also increases the gate leakage current, so a tradeoff between I_{ON} and I_{OFF} applies when varying t_{ox}, and one cannot use this approach to improve I_{ON} at the cost of I_{OFF}. The impact of high-k gate materials on the I_D–V_G characteristic of the heterogate JLTFET is shown in Fig. 6b, c, revealing a significant improvement in I_{ON} due to the reduction of λ with

high-k gate materials, as shown in Fig. 5a. One can observed from Fig. 6 that, by adopting a suitable high-k gate material, I_{ON}, I_{OFF}, and the subthreshold slope (calculated by Eq. 2) can be improved [5]. The average subthreshold slope for high-k gate materials HfO_2 ($k = 25$), La_2O_3 ($k = 30$), and TiO_2 ($k = 80$) was 48.2, 47.2, and 43.9 mV/dec, respectively. However, Si_3N_4 ($k = 7.0$), Al_2O_3 ($k = 9.0$), and Y_2O_3 ($k = 13$) showed average subthreshold slope (SS) of 103.4, 75.6, and 59.0 mV/dec, respectively.

The I_{ON} value for the simulated device was 7.2×10^{-7}, 1.2×10^{-6}, and 2.0×10^{-6} A/μm for high-k gate dielectric materials HfO_2 ($k = 25$), La_2O_3 ($k = 30$), and TiO_2 ($k = 80$), respectively. The leakage current at $V_{GS} = 0.0$ V varied from $\sim 10^{-15}$ to $\sim 10^{-14}$ A/μm for Si_3N_4 ($k = 7.0$), Al_2O_3 ($k = 9.0$), Y_2O_3 ($k = 13$), HfO_2 ($k = 25$), La_2O_3 ($k = 30$), and TiO_2 ($k = 80$) [27,28]. However, I_{OFF} for TiO_2 was $\approx 10^{-14}$ to 10^{-13} A/μm. Investigation of the device with high-k dielectric materials such as HfO_2 ($k = 25$), La_2O_3 ($k = 30$), and TiO_2 ($k = 80$) revealed I_{ON}/I_{OFF} ratios of $\approx 10^8$ for optimized device parameter combinations. The gate work functions Φ_m, Φ_{m1}, and the source/channel/drain doping were taken as 4.2 eV, 5.2 eV, and 1×10^{19}/cm^3, respectively.

$$SS = V_{DD}/\log_{10}\left(I_{ON}/I_{OFF}\right). \tag{7}$$

3.2 Impact of gate work function

Figure 7a, b shows the change in the energy-band diagram for the device when varying Φ_m to 4.1, 4.2, 4.3, 4.4, and 4.5 eV for Φ_{m1} of 5.2 eV. The effect of Φ_m on I_D–V_G is shown in Fig. 7c. A lower gate work function (Φ_m) results in more band bending in the channel near the source–channel junction [29–31], which helps to improve the I_{ON} characteristics of the device, as shown in Fig. 7.

This also increases I_{OFF}, as shown in Fig. 8. In OFF-state, lower Φ_m values ($4.1\,\text{eV} \le \Phi_m \le 4.5\,\text{eV}$) move the band downward in the channel region, as shown in Fig. 7a. This leads to an increase in the OFF-state I_{OFF} value of the simulated device, as shown in Fig. 8. The simulated ON-state band diagram in Fig. 7b shows a larger Φ_m value, bending the band along the channel. This occurs due to coupling between the gate and channel. This reduces the tunneling probability and increases the threshold voltage (V_{TH}), leading to the reduction of I_{ON} seen in Fig. 8.

Furthermore, the impact of the auxiliary gate work function (Φ_{m1}) of the heterogate JLTFET was investigated in detail. To do this, the auxiliary gate Φ_{m1} was varied to 5.1, 5.2, 5.3, 5.4, and 5.5 eV while keeping Φ_m constant at 4.2 eV. The OFF-state and ON-state and the I_D–V_G characteristic of the simulated device are shown in Fig. 9. Figure 9a, b shows the change in the band diagram versus Φ_{m1} while keeping Φ_m at 4.2 eV. As Φ_{m1} is increased, the tunneling width (λ) also increases, resulting in lower I_{ON} as well as I_{OFF}. This is due to the higher Φ_{m1} value pushed upward along the channel, as shown in Fig. 9a.

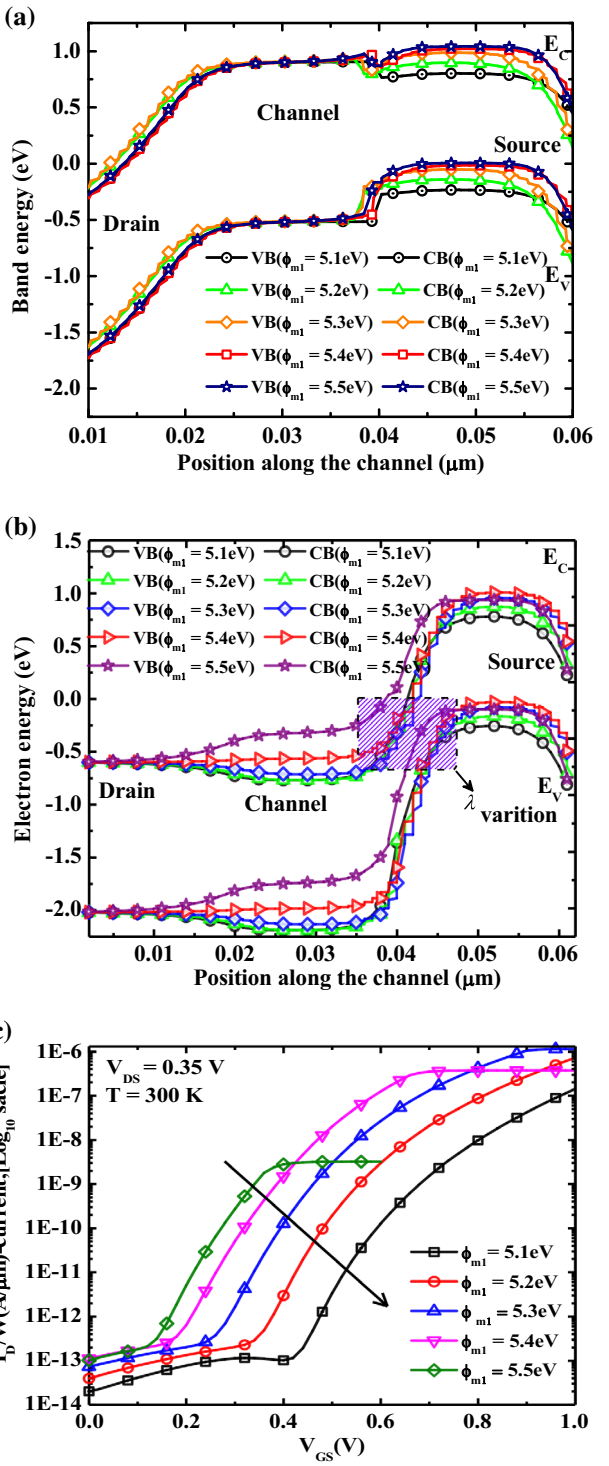

Fig. 9 Effect of auxiliary gate work function (Φ_{m1}) on the band diagram in **a** the OFF-state and **b** the ON-state, and **c** the I_D–V_G characteristic

Table 1 Average subthreshold slope of the simulated device in Fig. 1 with HfO_2 for $V_{DS} = 0.35$ V

S. no.	Group 1			Group 2		
	Control gate work function, Φ_m (eV)	Auxiliary gate work function, Φ_{m1} (eV)	Average subthreshold slope (mV/dec)	Control gate work function, Φ_m (eV)	Auxiliary gate work function, Φ_{m1} (eV)	Average subthreshold slope (mV/dec)
1	4.1	5.2	48.7	4.2	5.1	52.0
2	4.2	5.2	48.2	4.2	5.2	48.2
3	4.3	5.2	49.5	4.2	5.3	48.6
4	4.4	5.2	50.8	4.2	5.4	53.6
5	4.5	5.2	52.0	4.2	5.5	77.8

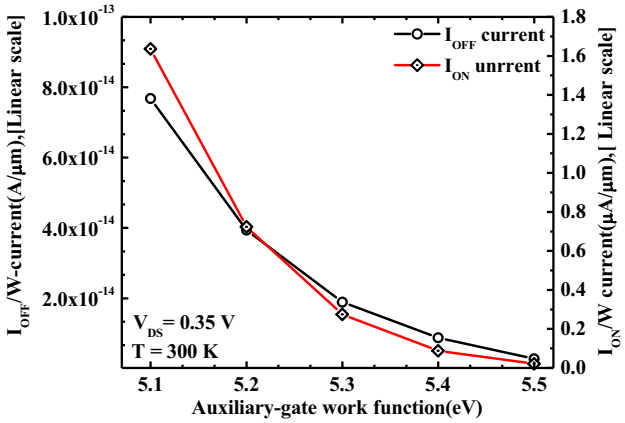

Fig. 10 I_{ON}, I_{OFF} current variation for the considered device when varying the auxiliary gate work function (Φ_{m1}) with $N_d = 1 \times 10^{19}/cm^3$, $t_{ox} = 2$ nm, $t_{spacer} = 5$ nm, and $\Phi_m = 4.2$ eV

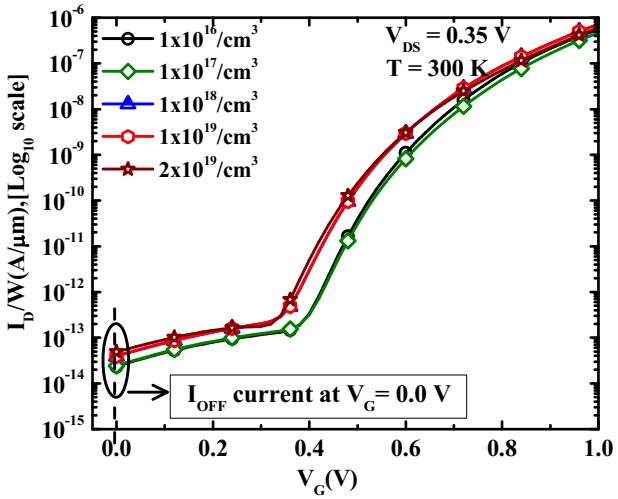

Fig. 11 Effect of doping on the transfer characteristics of the considered device in source/channel/drain

Table 1 summarizes the average subthreshold slope values extracted for different Φ_m and Φ_{m1} values. For work functions of 4.2 and 5.2 eV, the considered device showed optimized performance. The variation of I_{ON} and I_{OFF} versus the auxiliary gate work function Φ_m is shown in Fig. 10.

4 Impact of doping

This section is dedicated to the impact of doping variation on the device. To see the influence of source/channel/drain doping in the heterogate JLTFET, we used various uniform doping profiles of source/channel/drain, such as 1×10^{16}, 1×10^{17}, 1×10^{18}, 1×10^{19}, and $2 \times 10^{19}/cm^3$. The I_D–V_G characteristics of the heterogate JLTFET for the different doping levels are shown in Fig. 11. For the simulations shown in Fig. 11, we used Φ_m, Φ_{m1}, V_{DS}, and V_{G1} values of 4.2 eV, 5.2 eV, 0.35 V, and 0.0 V, respectively. The I_{ON} and I_{OFF} currents for the simulated device for these different doping levels are presented in Table 2. The variation of I_{ON}/I_{OFF} and the average subthreshold slope for the investigated doping range is shown in Fig. 12. The considered device showed a small variation for doping of 1×10^{16}, 1×10^{17}, 1×10^{18}, and $1 \times 10^{19}/cm^3$. However, doping the adopted device with $N_d > 1 \times 10^{19}/cm^3$ is not useful due to its limited I_{ON}/I_{ON} ratio. The subthreshold slope also starts to increase rapidly for $N_d > 1 \times 10^{19}/cm^3$, as shown in Fig. 10.

Table 2 Electrical parameters extracted for the simulated device

S. no.	Doping (cm^{-3})	I_{OFF} (A/μm)	I_{ON} (A/μm)
1	1×10^{16}	2.3×10^{-14}	5.5×10^{-7}
2	1×10^{17}	2.4×10^{-14}	4.7×10^{-7}
3	1×10^{18}	3.9×10^{-14}	7.2×10^{-7}
4	1×10^{19}	3.9×10^{-14}	7.2×10^{-7}
5	2×10^{19}	4.8×10^{-14}	6.0×10^{-7}

5 Conclusions

A detailed study of the heterogate JLTFET using the displacement vector concept is reported based on two-dimensional (2-D) simulations. The results demonstrate that the wide range of heterogate dielectric materials can enable mod-

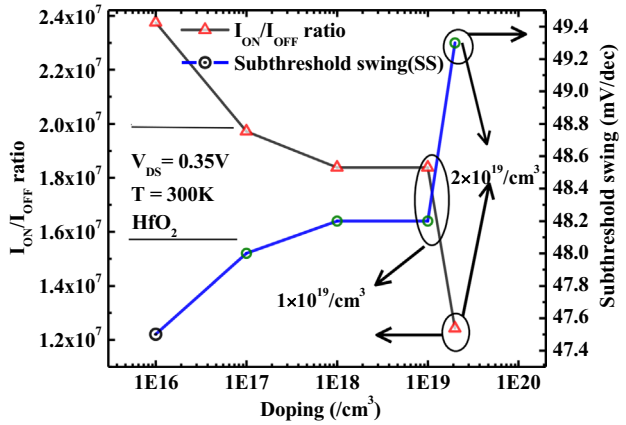

Fig. 12 Influence of doping profile on the I_{ON}/I_{OFF} ratio and average subthreshold slope at $V_{GS} = 1.0\,V$ and $t_{ox} = 2\,nm$

ulation of the device characteristics. The applied method provides high performance and high electric field in the heterogate JLTFET as a result of the combination of high-k and low-k dielectric materials. In summary, a new high-performance heterogate JLTFET is studied thoroughly, offering simulated results including $I_{ON} \approx 1.2 \times 10^{-6}\,A/\mu m$ and $I_{OFF} \approx 10^{-14}\,A/\mu m$ for La_2O_3. $I_{ON}/I_{OFF} \approx 10^8$ and subthreshold slope of $\approx 47.2\,mV/dec$ were obtained for the same dielectric. The performance of the heterogate JLTFET is mainly governed by the internal electric field inside the channel. Use of heterogate dielectric materials results in improved electric field. Use of high-k gate material improves I_{ON}, I_{OFF}, as well as the subthreshold slope of the device, while low-k gate material results in low I_{ON} and also degrades the subthreshold slope. It is also observed that, by changing the gate dielectric, the subthreshold slope can be modulated.

Work function engineering of gate materials also plays a significant role in modulating the threshold for charge tunneling from source to channel. Detailed study of the work function is also presented herein. Moreover, bandgap narrowing due to the high doping level in the device is also studied.

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