Temperature effect on hetero structure junctionless tunnel FET

Shiromani Balmukund Rahi[1,†], Bahniman Ghosh[1,2], and Bhupesh Bishnoi[1]

[1]Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India
[2]Microelectronics Research Center, 10100, Burnet Road, Bldg. 160, University of Texas at Austin, Austin, TX, 78758, USA

Abstract: For the first time, we investigate the temperature effect on AlGaAs/Si based hetero-structure junctionless double gate tunnel field effect transistor. Since junctionless tunnel FET is an alternative substitute device for ultra scaled deep-submicron CMOS technology, having very good device characteristics such as an improved subthreshold slope (< 60 mV/decade at 300 K) and very small static leakage currents. The improved subthreshold slope and static leakage current confirms that it will be helpful for the development of future low power switching circuits. The 2-D computer based simulation results show that OFF-state leakage current is almost temperature independent for the proposed device structure.

Key words: TFET; subthreshold slope (SS); temperature effect; band-to-band tunneling
DOI: 10.1088/1674-4926/36/3/034002 **EEACC:** 2570

1. Introduction

Tunnel FETs are one of the suitable candidates for fast switching applications in low power VLSI circuits design. The advantage of these devices is the possibility to obtain a subthreshold slope lower than conventional MOSFET (< 60 mV/decade) at room temperature, whereas 60 mV/decade is the thermodynamic limit of conventional MOS devices[1−4]. TFET is often realized as a gated p–i–n homojunction device[4, 5], which operates in reverse biased condition. The current conduction mechanism of TFETs is completely different from conventional MOSFETs. As there is band-to-band-tunneling (BTBT) of charge carriers in TFET, whereas in MOSFET, there is drift–diffusion of charge carriers[1−9].

Junctionless-tunnel field effect transistors (JL-TFETs) have been extensively studied in past few years[1−9]. Although JL-TFETs show better electrical performance and less variability than conventional MOSFETs because there are no p–n junctions. However, for their better device performance low band-gap heterostructure, channel JL-TFETs[3−12] are attracting more attention nowadays.

In this work, heterojunction engineering is incorporated with AlGaAs alloy and silicon, afterward band engineering is merging with the junctionless property for tunnel FETs. The inherent property of most all semiconductors to show temperature dependence energy band reduction which influences the device performance with temperature variations. In our work, AlGaAs/silcon semiconductor materials are used in the heterostructure source/channel, so we focused the temperature effect on the device performance for the first time. Rigorous investigation of device performance with temperature is done with a standard virtual device fabrication lab with Silvaco.

2. Device structure and simulation approach

Figure 1 shows a schematic view of the horizontal heterostructure junctionless double gate tunnel FET (HJL-DG TFET). Basically, the HJL-TFET is a double gated, uniform doped N-type structure. The device structure is also derived from fundamental p–i–n diode[10]. As shown in Figure 1, the source terminal of the device is attached to low band-gap silicon (1.12 eV at 300 K) and the drain terminal is connected with large band-gap AlGaAs ($\simeq$ 1.42 eV). The ON-current ($I_{\rm ON}$) in TFET depends on the transmission probability of electrons from the valence band of the source to the conduction of the channel[11]. This transmission probability can be modeled with the help of the Wentzel–Kramer–Brillouin (WKB) approximation[11−15].

$$T_{\rm WKB} \simeq \exp\left[-\frac{4\lambda\sqrt{E_{\rm G}^3}\sqrt{2m^*}}{3q\hbar(E_{\rm G}+\Delta\Phi)}\right]. \quad (1)$$

Here

$$\lambda = \sqrt{(\varepsilon_{\rm Si}/\varepsilon_{\rm ox})\, t_{\rm Si} t_{\rm ox}}. \quad (2)$$

In Equations (1) and (2), m^* is the effective mass, $E_{\rm G}$ is the bandgap, q is the electronic charge, and $\hbar$ is the reduced Planck constant. The symbol λ is the screening tunneling length (STL) and it depends on the specific device geometry. $\Delta\Phi$ is the difference in energy between the conduction band in the source

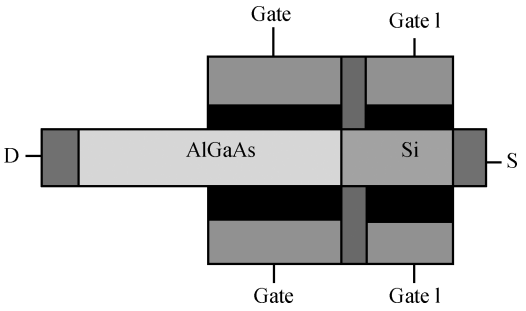

Figure 1. Cross-section of heterostructure junctionless double gate TFET (HJL-DG FET). In this structure, silicon (right) is attached to the source contact, while AlGaAs (left) is attached to the drain contact.

† Corresponding author. Email: sbrahi@gmail.com, sbrahi@iitk.ac.in
Received 28 March 2014, revised manuscript received 22 September 2014

Table 1. Parameters used in simulation.

Material	$E_G(0)$ (eV)	α (10^{-4} eV/K)	β (K)
Silicon	1.170	4.73	636

and the valence band in the channel. Generally, a low band-gap material is used in the traditional TFET structure for improving the ON-current (I_{ON})[16–20].

3. Band-gap reduction in heterostructure junctionless double gate TFET (HJL-DG TFET)

Low band gap semiconductors at the source side in TFET have been proposed to improve the I_{ON} current. The principal advantages of low band gap materials on the source side are an improvement in the ON-current, a suppression of the leakage current as well as a low OFF current[21, 22]. Temperature is one of the important stimuli affecting the band-gap of most of semiconductors. This physical parameter indirectly affects the device performance and hence, in this work, we focused on investigation of the device performance with temperature variation. Band-gap narrowing with temperature is dealt with in References [17–20, 23–25].

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T+\beta}, \tag{3}$$

where $E_G(0)$ is the extrapolated value of the band-gap at 0 K and α, β are fitting parameters. The typical values of parameters for silicon are listed in Table 1.

Energy band-diagram of uniformly doped N-type heterostructure junctionless tunnel FET at thermal equilibrium is shown in Figure 2. As shown in Figure 2, due to the different band-gap, there are discontinuities in the energy band as the Fermi level lines up in thermal equilibrium. Here ΔE_C, ΔE_V are conduction and valence band offsets, respectively.

The switching operation of HJL-DG TFET is usually controlled in two conduction states: OFF-state ($V_{GS} \simeq 0$ V) and ON-state ($V_{GS} > 0.0$ V). Energy band diagram of the same structure under non-equilibrium is also shown in Figure 2(b). As shown in Figure 2(b), in OFF-state, the potential barrier width between the source and the channel is too large and hence no tunneling occurs and only a very small leakage current due to thermionic emission. In ON-state, when the gate voltage is sufficiently large that the potential barrier between the source and the channel becomes narrow enough to allow a significant tunneling current.

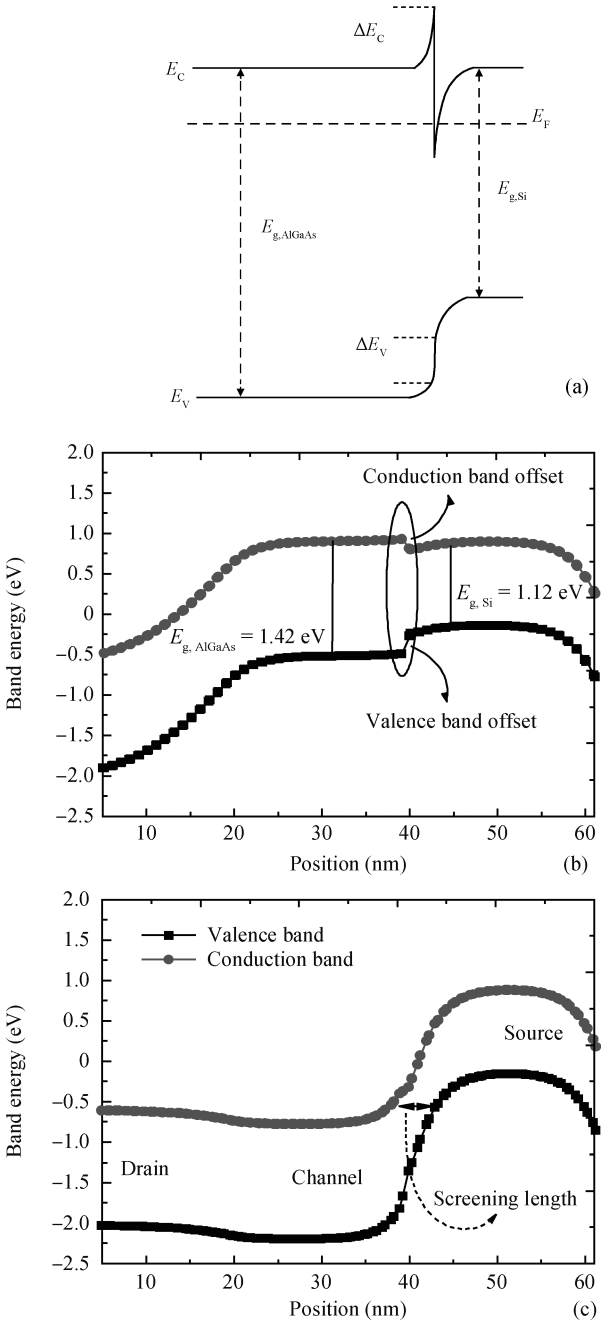

Figure 2. Band diagram of uniformly n-doped hetero structure JL-DG TFET at 300 K. (a) Equilibrium band-diagram. (b) OFF-state. (c) ON-state.

4. Band-to-band-tunneling current modeling approach and temperature dependency

HJL-DG FET is a quantum mechanical device. Current flow in HJL-DG TFET is due to band-to-band-tunneling (BTBT) of electrons from the valence band of the source to the conduction band of the channel. This BTBT current can be modeled using Kane's Model as follows[26–32].

$$I_{DS} = A_{Kane} D^2 E_G^{-0.5} V_{GS}^2 \exp\left(-B_{Kane} E_G^{1.5} / V_{GS} D\right). \tag{4}$$

Here D, A_{Kane} and B_{Kane} are constants and E_G is the band gap energy. Differentiating Equation (4) with respect to E_G, we get,

$$(\partial I_{DS}/\partial E_S) = -0.5 A_{Kane} D V_{GS} \exp\left(-B_{Kane} E_G^{1.5}/V_{GS}\right) \times \left(D E_G^{-1.5} + 3B_{Kane}\right). \tag{5}$$

Equations (3) and (5) show the drain-current dependence on the band-gap as well as the temperature.

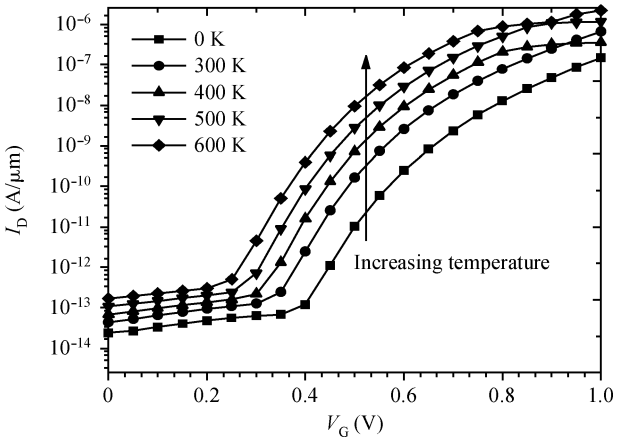

Figure 3. I_D–V_G characteristics of HJL-DG TFET with gate voltage ranging from 0 –1.0 V for the temperature range 0–600 K at V_{DS} = 0.35 V, T_{ox} = 2 nm.

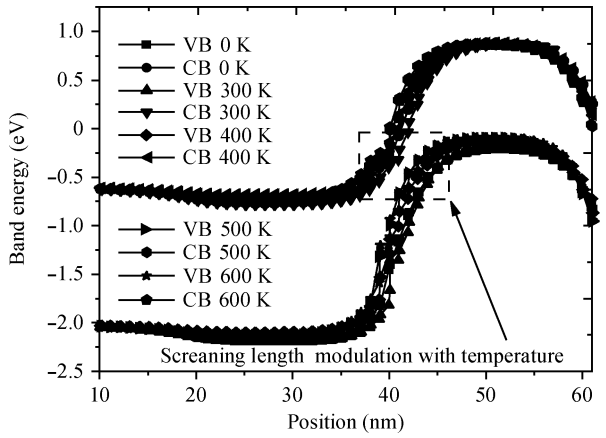

Figure 4. Screening length modulation with temperature for AlGaAs/Si based HJL- DGTFET. VB and CB stand for valance band and conduction band, respectively.

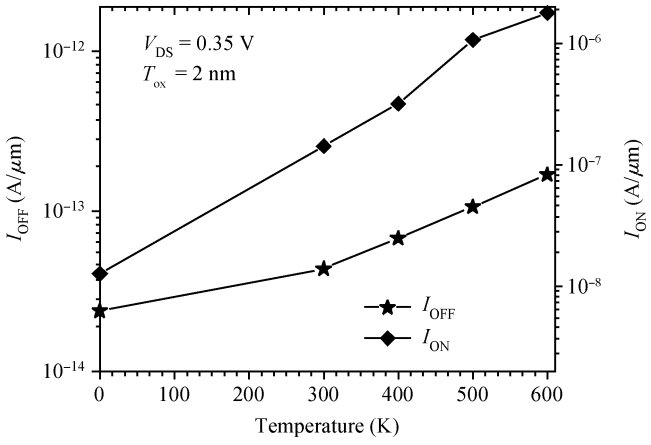

Figure 5. I_{ON}–I_{OFF} variation with temperature for V_{DS} = 0.35 V at 0–600 K.

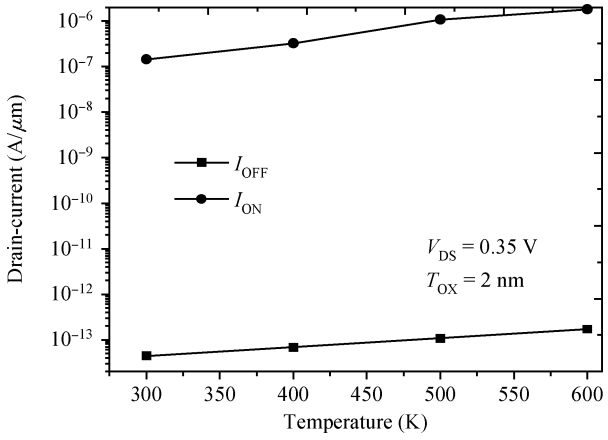

Figure 6. I_{ON}–I_{OFF} variation with temperature for V_{DS} = 0.35 V at 300–600 K.

5. Results and discussions

Figure 3 shows the simulated I_D–V_G characteristics of N-channel HJL-DG TFET operating in the temperature range of 0 to 600 K. The temperature effect on the drain-current is modeled in Sections 3 and 4 with the help of Equations (3)–(5). Equation (3) shows that the band-gap of silicon is a weak function of the temperature. The influence of temperature on the drain-current is shown in Figure 3. Qualitatively from this figure, it is observed that for a large range of temperature, a very small leakage current ($\simeq 10^{-14}$ to 10^{-13} A/μm) is obtained. So, HJL-TFET can be easily used at large ($\simeq$ 300 to 600 K) temperatures.

The screening tunneling length (λ) is one of the most significant parameters, which helps us to understand the band-to-band tunneling (BTBT) operation in TFET devices. BTBT is governed by WKB tunneling approximation and is formulated by Equation (1)[15, 18]. The tunneling probability of an electron from the valence band of the source to the conduction band of the channel is a weak function of temperature[12]. The same result is obtained in our study, as shown in Figure 4. For a large range of operating temperatures (0 to 600 K), very small variation in λ is obtained (see Figure 4), and this is directly related to the tunneling probability by Equation (1).

The carrier transport in HJL-DG TFET is dictated by B2B tunneling at the channel-source interface. Increasing the gate voltage pulls down the channel conduction band. This reduces the screening length and increases the tunneling probability. In OFF-state ($V_{GS} \leqslant 0$), the tunneling barrier is so large that electron tunneling is almost negligible. A very small thermally generated leakage current, I_{OFF}, is obtained. Figure 5 shows the variation of ON-current (I_{ON}) and OFF-current (I_{OFF}) for the temperature range 0–600 K, and Figure 6 shows the same variation for the range 300–600 K. From these two figures, it is clear that the leakage current is almost constant for temperature 0–600 K. Thus HJL-DG TFET can be operated for a larger temperature than 300 K. Tunnel FETs are expected to show weak dependence of I–V characteristics on temperature[28]. Similar results are observed in our study also.

For digital applications, a low I_{OFF} and a large I_{ON}/I_{OFF} ratio are desired. The I_{ON}/I_{OFF} ratios and their dependence on temperature are shown in Figures 7 and 8 for temperature ranges 0–600 K and 300–600 K respectively. The reverse leakage current in TFET slightly increases with temperature but it is a very weak function of temperature. A slight variation of I_{ON}

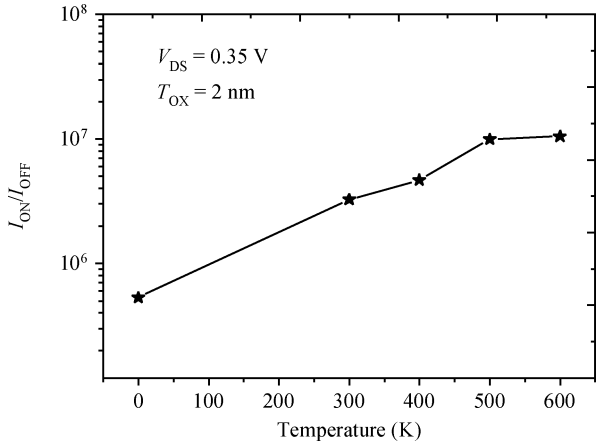

Figure 7. I_{ON}/I_{OFF} ratio variation with temperature at $V_{DS} = 0.35$ V for 0–600 K.

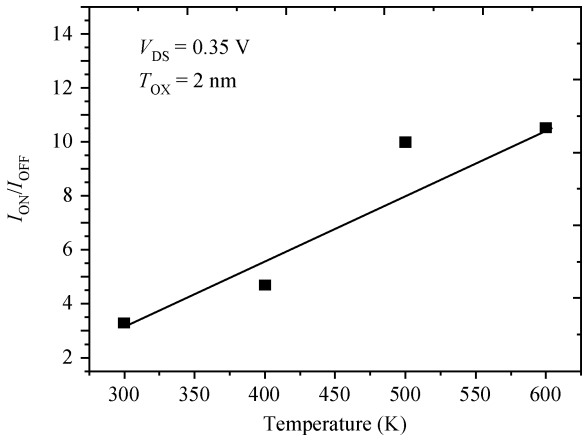

Figure 8. I_{ON}/I_{OFF} ratio variation with temperature at $V_{DS} = 0.35$ V at 300–600 K.

and I_{OFF} currents with temperature causes weak dependence of I_{ON}/I_{OFF} ratios on the temperature. Qualitatively, the temperature effect on the heterostructure junctionless tunnel TFET can be ignored due to weak dependency.

The variations of the extracted point subthreshold and average subthreshold slopes with temperature are shown in Figure 9 for HfO_2. The point subthreshold slope ($S_{point} \simeq$ 49 mV/decade) is smaller than in classical MOSFET ($\simeq$ 60 mV/decade). In Figure 9 the S_{avg} is weak function of E_G and is calculated by[5]

$$S_{avg} = \frac{V_T - V_{GOFF}}{\lg(I_T/I_{OFF})} \simeq \frac{V_{DD}}{\lg(I_{ON}/I_{OFF})}. \quad (6)$$

Here $V_{DD} = 0.35$ V. It is clear from Figure 9 that a slight variation of the sub-threshold slope with temperature degrades the switching characteristics. However, HJL-DG TFET has better temperature stability than classical MOSFET, showing improved subthreshold slope, low leakage and I_{ON} current[6].

6. Conclusion

In this paper, we rigorously investigated the device performance with temperature variation. During device investiga-

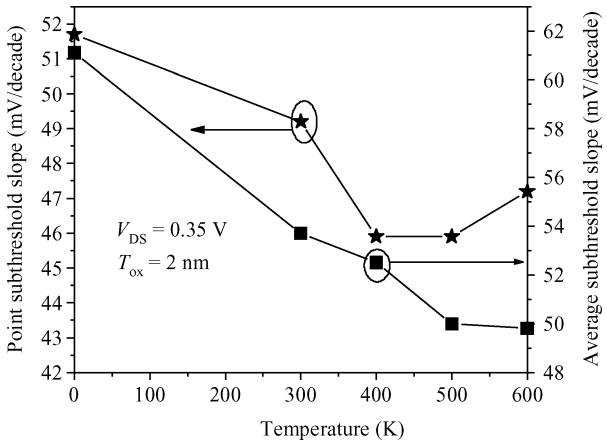

Figure 9. Subthreshold slope variation with temperature.

tion, it is that observed that the device characteristics of HJL-DG TFET is almost temperature independent for a large temperature range, 0–600 K. The device shows very small variation of I_{OFF} current (10^{-14}–10^{-13} A/μm) for the temperature range 0–600 K and point subthreshold slope variation around 48–46 mV/decade for temperature (300 to 600 K) as well as I_{ON} variation around 10^{-7} –10^{-6} A/μm for temperature 300–600 K. This investigation identified that AlGaAs/Si based heterostructure junctionless double gate tunnel FET (HJL-DG FET) shows almost temperature independent characteristics, which strongly support the published results[12]. Simulation results show that heterostructure junctionless tunnel FET (HJL-DG FET) is a promising device for applications involving temperatures as high as 300 K.

References

[1] Lattanzio L, Michiellis L D, Biswas A, et al. Abrupt switch based on internally combined band-to-band and barrier tunneling mechanisms. IEEE Proceedings of the European Solid-State Device Research Conference, 2010: 353

[2] Taur Y. An analytical solution to a double-gate MOSFET with undoped body. IEEE Electron Devices Lett, 2000, 21(5): 245

[3] Choi W Y, Park B G, Lee J D, et al. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett, 2007, 28(8): 743

[4] Ghosh B, Akram M W. Junctionless tunnel field effect transistor. IEEE Electron Device Lett, 2013, 34(5): 584

[5] Asthana P K, Ghosh B, Goswami Y, et al. High speed and low power ultra-deep-submicron III–V hetero-junctionless tunnel field effect transistor. IEEE Trans Electron Devices, 2014, 61(2): 479

[6] Bal P, Akram M W, Ghosh P M B. Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET). Springer, 2013

[7] Mammilla B K, Nair S, Mishra R, et al. A III–V group tunnel FETs with good switching characteristics and their circuit performance. International Journal of Electronics Communication and Computer Technology, 2011, 1(2): 26

[8] Asthana P K, Ghosh B, Rahi S B, et al. Optimal design of high performance H-JLTFET using HfO_2 as gate dielectric for ultra low power applications. RSC Adv, 2014, 43(4): 22803

[9] Rahi S B, Ghosh B, Asthana P. A simulation-based proposed high-k hetero structure AlGaAs/Si junction-less n-type tunnel FET. Journal of Semiconductors, 2014, 35(11): 114005

[10] Vadizadeh M, Faithipour M. Using low-k oxide for reduction of leakage current in double gate tunnel FET. IEEE 10th International Conference on Ultimate Integration of Silicon, 2009: 301
[11] Knoch J, Appenzeller J. A novel concept for field-effect transistors—the tunneling carbon nanotube FET. Proc 63rd DRC, 2005, 1: 153
[12] Boucart K, Ionesscu A M. Double-gate tunnel FET with high-k gate dielectric. IEEE Trans Electron Devices, 2007, 54(7): 1725
[13] Lattanzio L, Michielis L D, Biswas A, et al. Abrupt switch based on internally combined band-to-band and barrier tunneling mechanisms. IEEE Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2010: 353
[14] Knoch J. Optimizing tunnel FET performance-impact of device structure, transistor dimensions and choice of material. IEEE International Symposium on VLSI Technology, Systems, and Application, 2009: 45
[15] Ionescu A M, Riel H. Tunnel field-effect transistors as energy-efficient electronic switches. Nature, 2011, 479: 329
[16] Sze S M. Physics of semiconductor devices. 2nd ed. New York: Wiley, 1981: 15
[17] Green M. Intrinsic concentration, effective densities of states, and effective mass in silicon. J Appl Phys, 1990, 67: 2944
[18] Sze S M, Ng K K. Physics of semiconductor devices. 3rd ed. Wiley India Edition, 2011: 15
[19] Alex V, Finkbeiner S, Weber J. Temperature dependence of the indirect energy gap in crystalline silicon. J Appl Phys, 1996, 79: 6943
[20] Varshni Y P. Temperature dependence of the energy gap in semiconductors. Physica, 1967, 34(1): 149
[21] Nayfeh O M, Hoyt J L, Antoniadis D A. Strained-$Si_{1-x}Ge_x$/Si band-to-band tunneling transistors: impact of tunnel-junction germanium composition and doping concentration on switching behavior. IEEE Trans Electron Devices, 2009, 56(10): 2264
[22] Heyns M, Alian A, Brammertz G, et al. Advancing CMOS beyond the Si roadmap with Ge and III/IV devices. IEEE International Electron Devices Meeting (IEDM), 2011: 13.1.4
[23] Green M A. Intrinsic concentration, effective densities of states, and effective mass in silicon. J Appl Phys, 1990, 67: 2944
[24] Arora N. MOSFET modeling for VLSI simulation, theory and practice. World Scientific, 1992
[25] Van Zeghbroeck B. Principles of semiconductor devices. University of Colorado, 2007
[26] Kane E O. Zenner tunneling in semiconductor. J Phys Chem Solids, 1960, 12(2): 181
[27] Born M, Bhuwalka K K, Schinder M, et al. Tunnel FET: a CMOS device for high temperature applications. IEEE 25th International Conference on Microelectronics, 2006: 124
[28] Bhuwalka K K, Born M, Schinder M, et al. P-channel tunnel FET transistors down to sub-50 nm channel lengths. Jpn J Appl Phys, 2006, 45(4B): 3106
[29] Atlas User Manual. 19 December, 2013: 246
[30] Boucart K, Ionesscu A M. Double-gate tunnel FET with high-k gate dielectric. IEEE Trans Electron Devices, 2007, 54(7): 1725
[31] Lattanzio L, De Michielis L, Biswas A, et al. Abrupt switch based on internally combined band-to-band and barrier tunneling mechanisms. IEEE Proc of the European Solid-State Device Research Conference, Sevilla, Spain, 2010
[32] Hurkx G A M, Klasssen D B M, Knuvers P G. A new recombination model for device simulation including tunneling. IEEE Trans Electron Devices, 1992, 39(2): 331