Compact analytical model of double gate junction-less field effect transistor comprising quantum-mechanical effect

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Abstract: We investigate the quantum-mechanical effects on the electrical properties of the double-gate junction-less field effect transistors. The quantum-mechanical effect, or carrier energy-quantization effects on the threshold voltage, of DG-JLFET are analytically modeled and incorporated in the Duarte *et al.* model and then verified by TCAD simulation.

Key words: quantum-mechanical effect; junction-less transistor; threshold voltage; oxide thickness

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1. Introduction

The current generation of JLFETs undergoes noteworthy quantum mechanical effects (QME), because of the very high level of substrate doping and the very small oxide thickness in the range of nanometers. Due to these reasons, severe bending of the band on the substrate (Si) side takes place, which is due to the significantly high electric field existing at the interface. This results in a narrowing of the potential well, which is sufficient for energy quantization of carriers at the interface, because of which at the same gate bias, the inversion charge density gets reduced as compared to that predicted by classical theory. As a result, device parameters, like the threshold voltage, drain current, transconductance, etc., also change[1]. So the quantum mechanical behavior needs to be incorporated in compact JLFET models used for circuit simulations. Since threshold voltage plays an extremely important role in device characteristics, so in this paper, we have focused on the changes in threshold voltage and their effect on drain current due to the QM effect.

2. Junction-less field effect transistor

A conventional MOSFET is made up of two p–n junctions, one at the source and the other at the drain region. As devices are down scaled in accordance with Moore's law, a large doping concentration gradient and careful fabrication are required for the formation of such junctions in order to avoid punch through. These rigorous demands have pushed the scaling of their fundamental limits. Therefore, a new device, a junction-less (JL) transistor, has been proposed to solve the above mentioned problems, as shown in Figure 1.

Although the structure of JLFET and conventional MOSFET are very much similar, but with homogeneous doping polarity and uniform doping concentration across the device, there is no junction formation and that is why they are called junction-less FETs. The primary conduction mechanism in a JLFET depends on the bulk current not on the surface; moreover, in turning it off, the channel needs to be fully depleted. When the gate voltage is below V_{TH}, the channel gets fully depleted and the device is in a sub-threshold state. As the gate voltage increases gradually and becomes equal to V_{TH}, the channel gets partially depleted and so current flows through the bulk condition mechanism. When the gate voltage exceeds the flat-band voltage, a complete neutral channel takes form and current can flow through the entire channel[2].

3. Quantum mechanical effects

Spatially confined channel carriers in one dimension, by either space confinement or electronic confinement, carrier-energy quantization, for DG JLFETs, becomes noteworthy. Thus, at a given gate bias, the QM inversion charge density is smaller than the classical one. So, one needs to apply more gate voltage to get the same value of inversion charge[3]. Solving self-consistently, via Gauss's law, shows a QM channel potential is lower than the channel potential in a classical one. The QM effect in the sub-threshold region of operation is defined by the difference between the two potentials.

4. Modeling of JLFET

Considering only mobile charges in the silicon region, the Poisson equation can be written using the Pao-Shah integral as:

$$\frac{\mathrm{d}^2\varphi}{\mathrm{d}x^2} = -\frac{qN_{\mathrm{si}}}{\varepsilon_{\mathrm{si}}}\left[1-\mathrm{e}^{(\varphi-V)/v_{\mathrm{t}}}\right], \tag{1}$$

where $\varepsilon_{\mathrm{si}}$ is the permittivity of silicon, φ is the channel potential, and V is the electron quasi-Fermi potential. Using

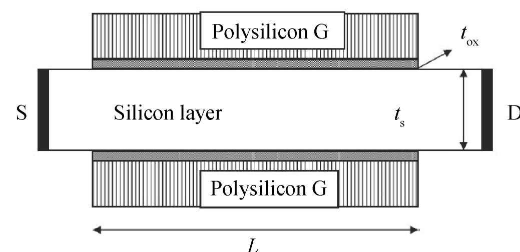

Figure 1. A junction-less transistor.

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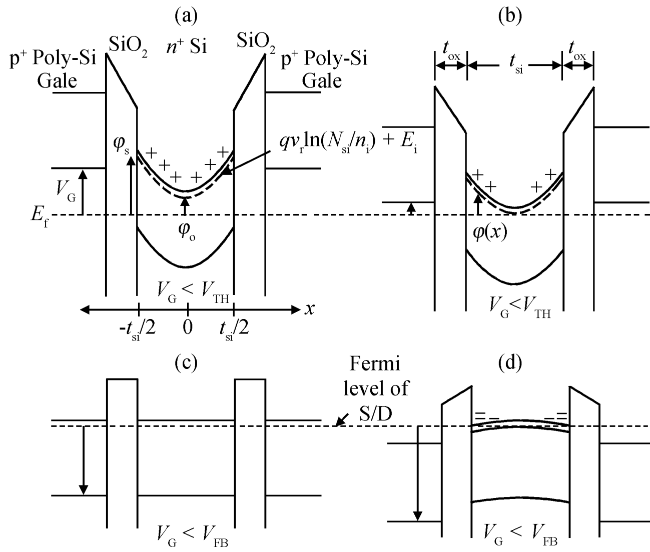

Figure 2. Schematic band diagrams for a symmetric DG-JLFET. (a) Fully depleted and downwardly bent channel in the sub threshold mode. Partially depleted and downwardly bent channel in the bulk current mode. (c) Flattened channel in the flat band mode. (d) Upwardly bent channel in the accumulation.

parabolic potential approximation, we obtained an analytical expression for the channel potential, which can be represented by:

$$\varphi(x) = (4x^2/t_{si}^2)(\varphi_s - \varphi_o) + \varphi_o, \quad (2)$$

where φ_o and φ_s are the potential at the center and the surface of the channel, respectively. Using Gauss law along with the boundary condition, we can determine the relationships between φ_s, φ_o, and the gate voltage V_G as:

$$-\frac{\varepsilon_{ox}}{t_{ox}}(V_G - V_{FB} - \varphi_s) = -\varepsilon_{si}\frac{d\varphi}{dx}|_{x=t_o/2} = \frac{4\varepsilon_{si}}{t_{si}}\Delta\varphi. \quad (3)$$

Here, ε_{ox} is the permittivity of the oxide, and $\Delta\varphi = \varphi_o - \varphi_s$. By approximating φ_o to zero at V_{TH} and assuming a fully depleted channel, a criteria for threshold voltage can directly be derived from the above equation, which is:

$$V_{TH} = V_{FB} - qN_{si}t_{si}t_{ox}/2\varepsilon_{ox} - qN_{si}t_{si}^2/8\varepsilon_{si} - qN_{si}t_{si}^2/0.16\varepsilon_{si}. \quad (4)$$

In the expression for V_{TH}, the last term is used as a fitting parameter, which is dependent on doping and silicon thickness. The total charges can be obtained by integrating the charge density over the entire channel, and subtracting fixed charges from that, we can obtain the total mobile charges by subtracting fixed charges from the total charge, which can be derived by integrating the charge density over the entire channel using the channel potential; a closed form of the expression for the mobile charge within the channel can be obtained, which is:

$$\frac{-2\varepsilon_{ox}}{\beta t_{ox}}(V_G - V_{TH} - V) = Q_{mobile} - \frac{2\varepsilon_{ox}v_T}{\beta t_{ox}}\ln\frac{-Q_{mobile}}{\sqrt{2\varepsilon_{si}\pi v_T q N_{si}}}. \quad (5)$$

A drain current expression can be derived by integrating the current continuity equation $I_{DS}\,dy = -\mu W Q_{mobile}dV$ from the source–drain region and expressing dV as $(dV/dQ_{mobile}) \times dQ_{mobile}$[4, 5],

$$I_{DS} = \mu\frac{W}{L}\int_0^{V_{DS}} Q_{mobile}dV, \quad (6)$$

$$I_{DS} = \mu\frac{W}{L}\left(\frac{\beta t_{ox}}{4\varepsilon_{si}}Q_{mobile}^2 - v_T Q_{mobile}\right)|_{Q_s}^{Q_D}, \quad (7)$$

where

$$\beta = 1 + \frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}. \quad (8)$$

The saturation drain voltage has been derived and it comes out to be:

$$V_{DS,Sat} = V_t\left\{1 - \lg\left[2v_T\varepsilon_{ox}/(\beta t_{ox}\sqrt{2\varepsilon_{si}\pi v_T q N_{si}}\right]\right\} + (V_G - V_{TH}). \quad (9)$$

Here, μ is the effective mobility, W is the device width, and L is the gate length.

5. Incorporation of QM effect

Because of the energy quantization of the carriers in a channel, the long-channel threshold voltage is anticipated to shift. Since, for a silicon crystal with a $\langle 100\rangle$ orientation, there are in total six valleys in the conduction band, which are clustered in two separate groups with degeneracy factors $g_1 = 2$ and $g_2 = 4$, respectively.

The threshold voltage after considering quantization is the gate voltage when the electron sheet density Q_{QM} reaches a threshold value Q_{TH}, which in the classical case can be expressed as $Q_{CL} = n_i t_{si}\exp(q\varphi_{CL}/kT)$ where φ_{CL} is the channel potential without considering the quantum mechanical effect referenced to the source Fermi level and it is constant throughout the channel thickness. The difference between φ_{QM} and φ_{CL} under a constant quantum mechanical effect gives the long-channel V_{TH} shift, ΔV_{TH} as there is a one-to-one relationship between the applied gate voltage and the channel potential[6, 7], so:

$$\Delta V_{TH,Long} = \frac{E_g}{2q}\ln n_i t_{si} - \frac{kT}{q} \times \ln\left[\sum_{i=1}^{2} g_i\frac{m_{D,i}^*}{\pi\hbar^2}kT\sum_j \exp\left(\frac{-E_{ji}}{kT}\right)\right]. \quad (10)$$

Here, E_g is the silicon band gap. $m_{D,i}^*$ $(i = 1, 2)$ are the density of states (DOS) effective masses of an electron, given as $m_{D,1}^* = m_t^*$, and $m_{D,2}^* = \sqrt{m_l^* m_t^*}$ where m_l^* and m_t^* are longitudinal and transverse effective masses of an electron, respectively. E_{ji} is the j-th sub-band in the i-th group of valleys given by:

$$E_{ji} = j^2(2\pi\hbar)^2/8m_{m,t}^* t_{si}^2, \quad (11)$$

where $m_{m,i}^*$ are motion effective masses of an electron, given as $m_{m,1}^* = m_l^*$ and $m_{m,2}^* = m_t^*$.

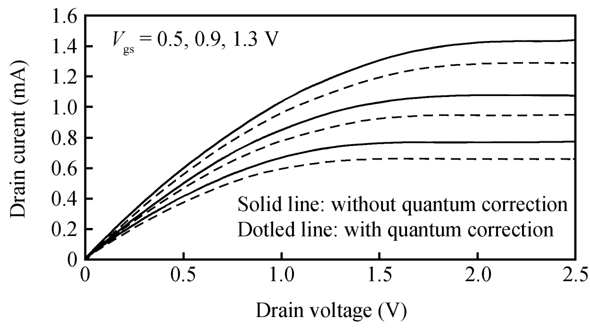

Figure 3. Plot showing QM effect on IV characteristics at different gate voltages.

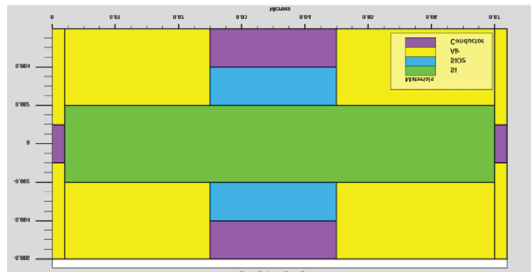

Figure 4. Junction-less FET.

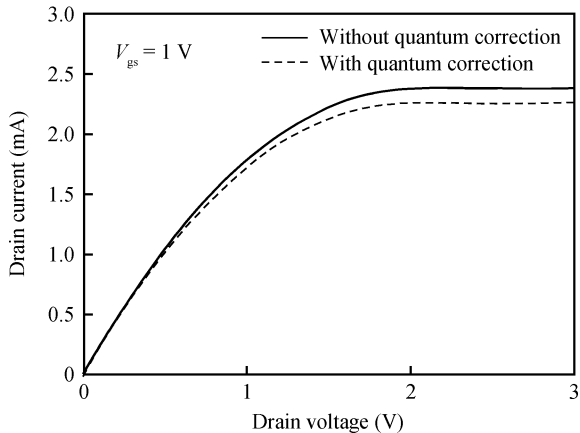

Figure 5. I_{ds} versus V_{ds} for t_{ox} = 2 nm and t_{si} = 4 nm.

6. Model validation

To confirm the proposed model, a numerical simulation using 2-D SILVACO has been carried out. The Shockley Read Hall Recombination model is used, which accounts for the field-dependence and doping effect. The Fermi–Dirac carrier statistics, along with band gap narrowing models, is used in the simulation. Throughout the simulations, the length of the channel and the width of the device are equal to 1 μm. In order to neglect the parasitic resistance effects, source and drain lengths are assumed to be very small.

The parameters and values used for SILVACO simulation are kept the same as those which are used in analytical modelling. The value of mobility used in the model was extracted from the linear region and it comes out to be around 110 $cm^2/(V{\cdot}s)$ for doping concentrations of 1×10^{18} cm^{-3}.

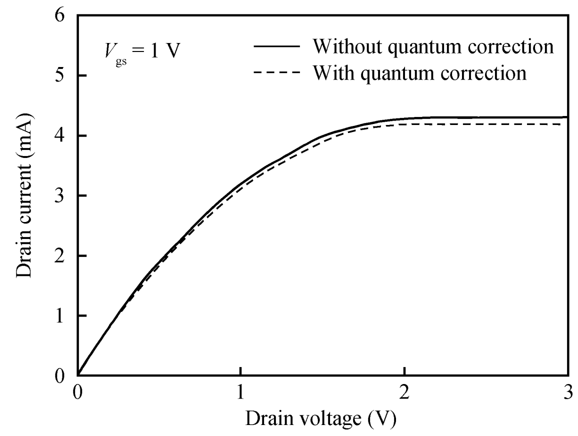

Figure 6. I_{ds} versus V_{ds} for t_{ox} = 2 nm and t_{si} = 8 nm.

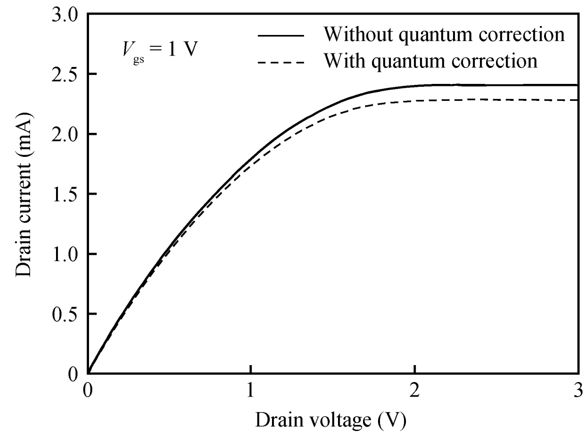

Figure 7. I_{ds} versus V_{ds} for t_{ox} = 4 nm and t_{si} = 4 nm.

Table 1. Dependence of change in threshold voltage to the silicon thickness.

Silicon thickness (nm)	Increase in threshold voltage (V)
2	0.1158
3	0.0690
4	0.0530
5	0.0420
10	0.0210

7. Simulation result

Figures 5–8 show the plot of drain current on the y-axis and the drain voltage of a double gate-JLFET on the x-axis, for different silicon and oxide thicknesses obtained from modeled data. Figures 9–12 show the drain current versus the gate voltage of double gate-JLFETs for different silicon and oxide thicknesses respectively obtained from modeled data. Figures 13–16 show the extent of matching between quantum corrected modeled data and simulated data I_{ds} versus V_{ds} data. Similarly, Figures 17–20 show the extent of matching between quantum corrected modeled data and simulated data of I_{ds} versus V_{gs}. In addition. Table 1 shows the dependence of change in threshold voltage to the silicon thickness.

From Table 1, we can see that as silicon thickness increases keeping the oxide thickness constant, the increase in threshold voltage decreases and for thickness above 10 nm, the increase

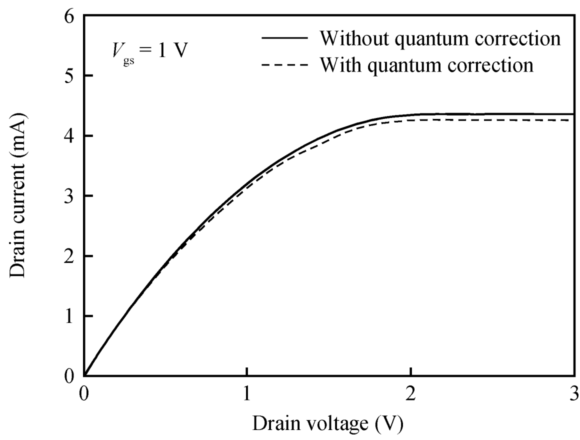

Figure 8. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 8$ nm.

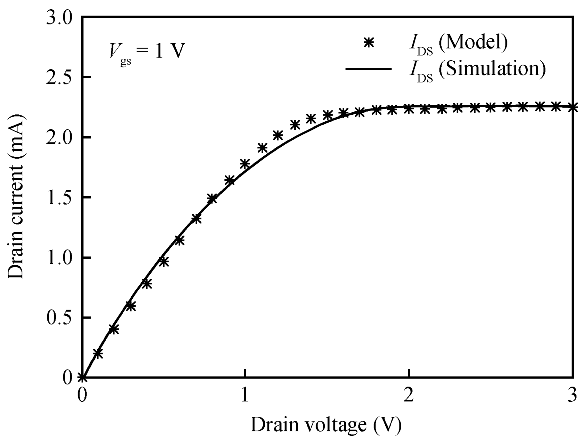

Figure 9. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 4$ nm.

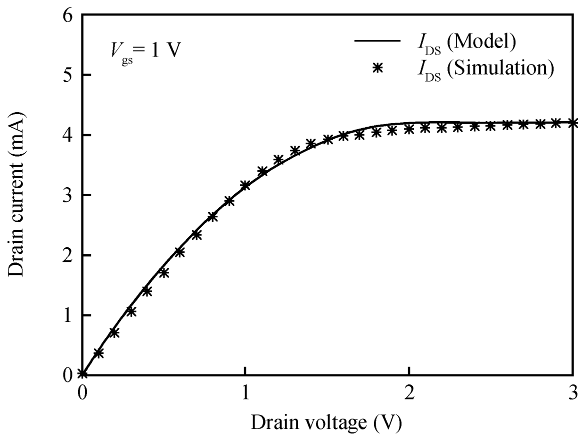

Figure 10. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 8$ nm.

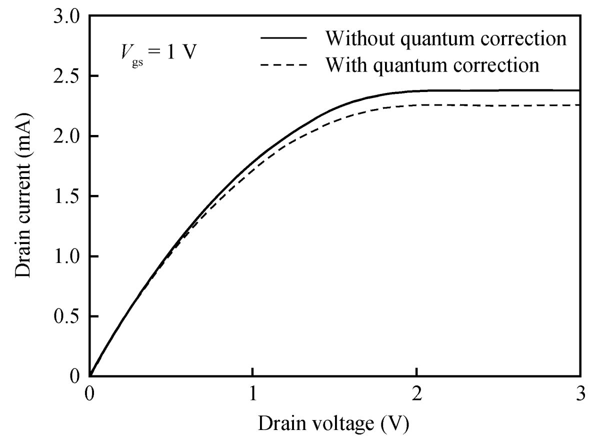

Figure 11. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 4$ nm.

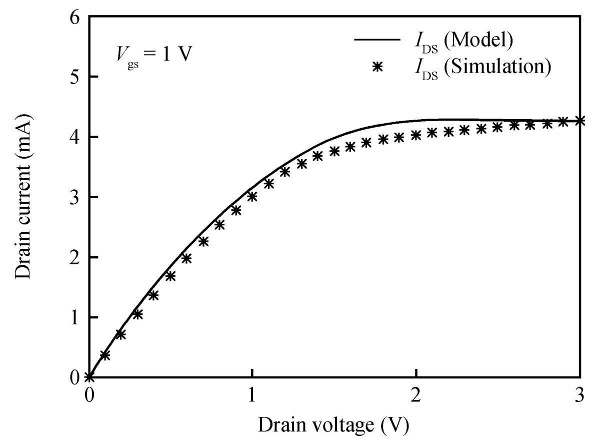

Figure 12. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 8$ nm.

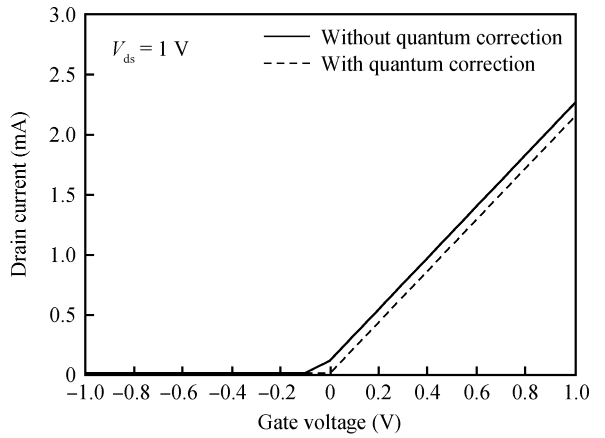

Figure 13. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 4$ nm.

is meniscus. An increase in threshold voltage leads to a decrease in the saturation current and trans-conductance.

8. Results

The satisfactory correlation between the proposed analytical model and the TCAD simulation results with some fitting parameters, which depend on silicon thickness and doping, confirm the proposed model. This model therefore continuously predicts the current characteristics of double gate JLFETs in the linear, saturation, and sub-threshold regions of operation.

9. Conclusion

In conclusion, the QM correction term for threshold voltage has been incorporated in continuous charge model. This model is developed for a DG-JLFET, which is symmetric and long channel. The Pao-Shah has been used and the parabolic

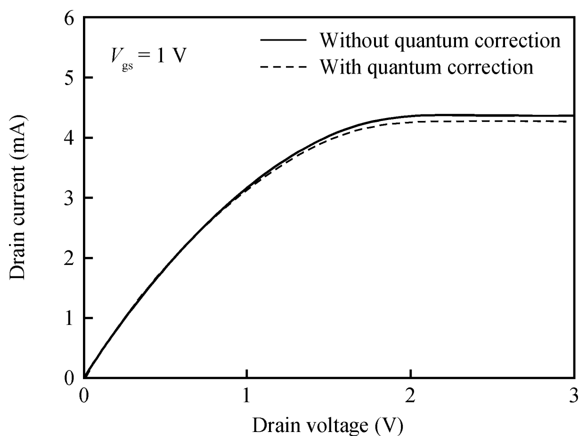

Figure 14. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 8$ nm.

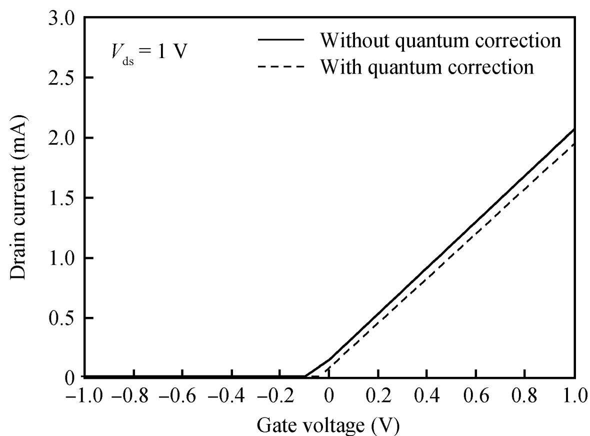

Figure 15. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 4$ nm.

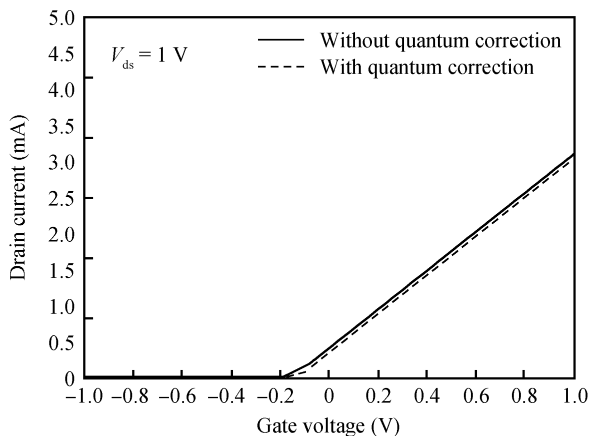

Figure 16. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 8$ nm.

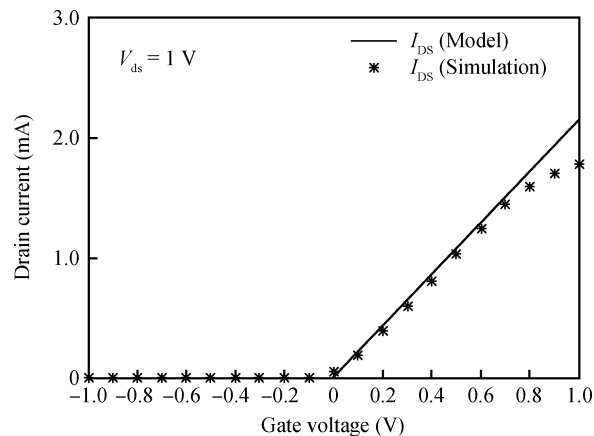

Figure 17. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 4$ nm.

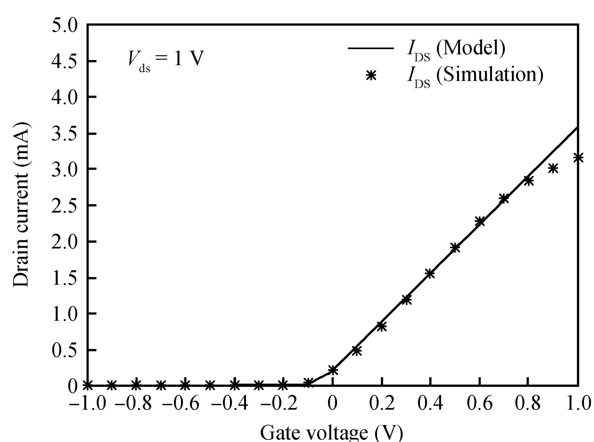

Figure 18. I_{ds} versus V_{ds} for $t_{ox} = 2$ nm and $t_{si} = 8$ nm.

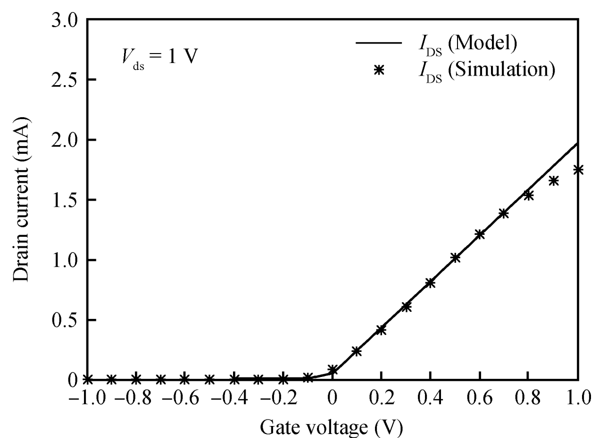

Figure 19. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 4$ nm.

potential approximation is extended to the sub-threshold and linear regions, which takes into account the mobile carrier charges and the dopant. The simulation results are then verified using SILVACO incorporating some fitting parameters.

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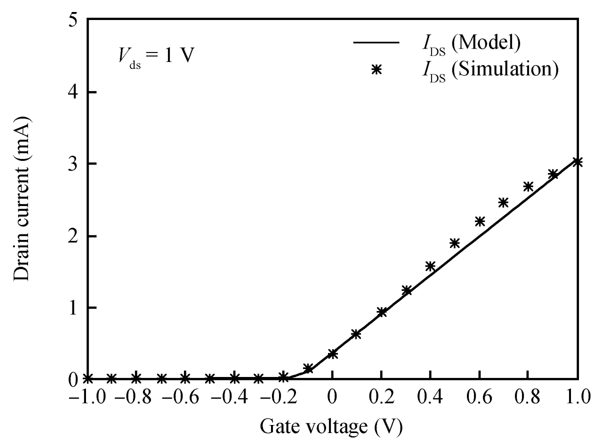

Figure 20. I_{ds} versus V_{ds} for $t_{ox} = 4$ nm and $t_{si} = 8$ nm.

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