A simulation-based proposed high-k heterostructure AlGaAs/Si junctionless n-type tunnel FET

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Abstract: We propose a heterostructure junctionless tunnel field effect transistor (HJL-TFET) using AlGaAs/Si. In the proposed HJL-TFET, low band gap silicon is used in the source side and higher band gap AlGaAs in the drain side. The whole AlGaAs/Si region is heavily doped n-type. The proposed HJL-TFET uses two isolated gates (named gate, gate1) with two different work functions (gate = 4.2 eV, gate1 = 5.2 eV respectively). The 2-D nature of HJL-TFET current flow is studied. The proposed structure is simulated in Silvaco with different gate dielectric materials. This structure exhibits a high on current in the range of 1.4×10^{-6} A/μm, the off current remains as low as 9.1×10^{-14} A/μm. So I_{ON}/I_{OFF} ratio of $\simeq 10^8$ is achieved. Point subthreshold swing has also been reduced to a value of $\simeq$ 41 mV/decade for TiO_2 gate material.

Key words: band-to-band tunneling (BTBT); TFET; heterostructure junctionless tunnel field effect transistor (HJL-TFET); I_{ON}/I_{OFF} ratio subthreshold slope; VLSI

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1. Introduction

As MOS technology extends toward nanometer range for future VLSI technology, MOS device dimensions are aggressively scaled. The purpose of aggressive scaling is to achieve high speed, low power consumption for highly dense VLSI circuits. Reduction of device dimensions, especially the oxide thickness below certain limits, enhances leakage currents. The enhanced leakage currents also enlarge the power consumption in ultra-scaled VLSI circuits. The tunnel field effect transistors (TFETs) are one of the leading candidates in nanoelectronics for ultra-low power applications because of their extremely small subthreshold swing (SS). Such subthreshold swing results in very low off-state leakage current and the device can be operated at much lower power supply voltage, resulting in reduction of power consumption in ultra dense VLSI circuits[1, 2].

Junctionless tunnel field effect transistors (JL-TFETs) are extensively studied in a lot of recent publications[3–9]. This is essentially because the subthreshold swings of JL-TFETs are significantly lower than 60 mV/decade[10, 11]; this is the limit of MOSFETs at room temperature. JL-TFETs are basically quantum mechanical devices based on band-to-band tunneling. Although JL-TFETs show better electrical performance and less variability than MOSFETs—because there are no p–n junctions—for better tunneling current, low band-gap hetero structure channel JL-TFETs[3–12] attracted attention.

Currently, significant attention is being paid to III–IV compound semiconductors rather than Si for improving the device characteristics such as low off current and higher on-current. In this paper, we propose a heterostructure channel based AlGaAs/Si junctionless TFET for investigating the device characteristics. First, heterojunction engineering is incorporated with AlGaAs alloy and silicon and afterwards band engineering is merged with junctionless property for TFETs.

2. Device structure and simulations

The proposed device structure studied in this paper is shown in Fig. 1. This work focused on an n-type device. In the proposed device structure all parameters used in simulations for AlGaAs/Si HJL-TFET are: gate length = 20 nm, gate dielectric thickness (T_{ox}) = 2 nm, film thickness (T_{si}) = 5 nm,

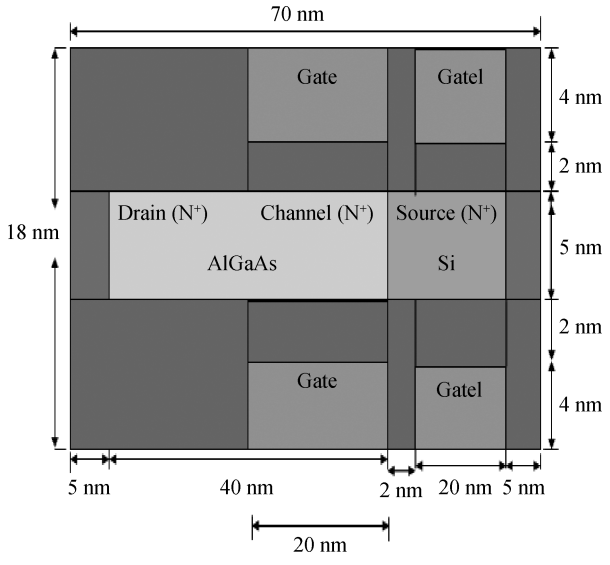

Fig. 1. Longitudinal cross section of proposed device structure of AlGaAs/Si HJL-TFET. The width of device equals to 1 μm. The work functions of gate (i.e. control gate) and gate1 (i.e. auxiliary gate) are 4.2 eV and 5.2 eV respectively.

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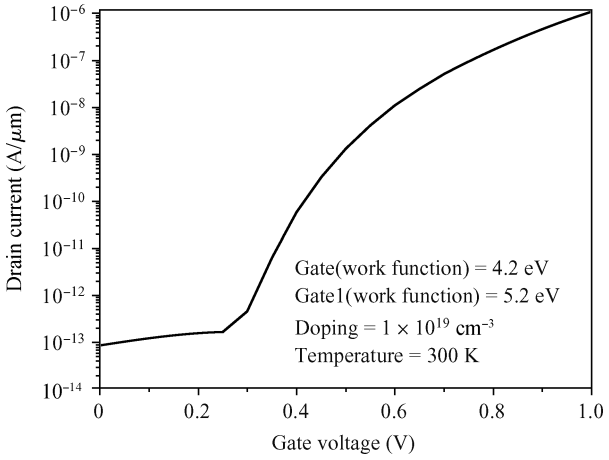

Fig. 2. I_D–V_G characteristics of proposed heterostructure JL-TFET at 300 K.

low-k spacer thickness = 2 nm, work function of poly n^+ region of gate = 4.2 eV, work function of poly p^+ region of gate1 = 5.2 eV, supply voltage = 1.0 V and carrier concentration in uniformly doped channel $N_D = 1.0 \times 10^{19}$ cm^{-3}.

All simulations are done in SILVACO ATLAS 2D V5.18.3 R. Shockley–Read–Hall (SRH) recombination, drift–diffusion current transport model, and Lombardi mobility model are used for simulations[13, 14]. Apart from that, the band gap narrowing (BGN) model is used because of the highly doped channel region[14]. Non-local band-to-band tunneling model is also included for studying the tunneling effect[6]. For further accuracy, Schenk's trap assisted tunneling (TAT) model and quantum confinement (QC) model are incorporated[13, 14].

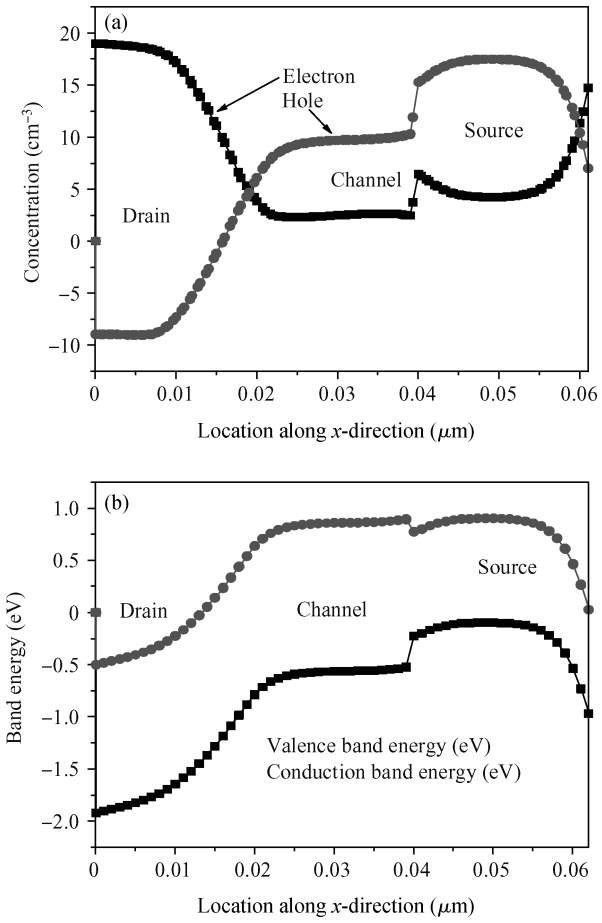

Fig. 3. (a) OFF-state electron and hole concentration of HJL-TFET. (b) OFF-state energy band diagram of HJL-TFET.

3. Basic physics and operation

Physics of tunnel FETs is quite different from that of classical MOSFETs. TFETs are quantum–mechanical devices and current flow in TFETs is governed by band-to-band-tunneling of charge carriers from the valence band of the source to the conduction band of the channel. The basic device operation is governed by controlling gate voltage (V_G). The device is commonly studied by simulation in two different regions: (1) OFF-state: when $V_G = 0.0$ V and (2) ON-state: when $V_G > 0.0$ V. In OFF-state, a very small leakage current flows from source to drain. In ON-state, applied gate (V_{G1}) voltage is sufficient to pull down conduction towards the valence band and barrier width is sufficiently minimized. The minimized barrier width due to applied voltage on the controlling gate ($V_G > 0.0$ V) terminal helps in band-to-band tunneling of charge carriers from source to drain. Thin dielectric stack gate material provides remarkable advantages as[9]: (1) it forbids thermionic emission from source to drain due to a very high potential barrier; (2) it provides remarkable band bending at low gate voltage; (3) it lowers the electron effective barrier height at high applied gate voltage[15, 19].

4. Results and discussion

The simulated HJL-TFET device structure is extracted from gated p–i–n diode. Figure 2 shows the I_D–V_G characteristics of the proposed heterostructure junctionless-TFET. Current is measured for large gate–source voltage (V_{GS}) for validity of device performance. Figure 3(a) represents the electron–hole concentration profile for simulated heterostructure junctionless TFET. From this figure it is observed that the device looks like n^+–i–p^+ doped structure. For OFF-state (i.e. $V_{GS} = 0.0$ V) energy band diagram is shown in Fig. 3(b). In OFF-state energy the band-diagram shows that the tunneling probability of the electron from the valence band of the source to the conduction of the channel is much less because of the large barrier width between the source and the channel and hence only a small leakage current flows in the device. By applying the appropriate voltage ($V_{GS} > 0.0$ V) on the control gate (i.e. Gate in device structure), HJL-TFET is turned ON, due to narrowing of the barrier between the source and the channel. In this situation the electron easily tunnels from the source to the channel in HJL-TFET.

In the case of the TFET, it is observed that the ON-current (I_{ON}) exponentially increases with a decrease of tunneling barrier width[20–23]. The ON-state energy band profile is shown in Fig. 4(a). Similarly the ON-state charge profile is shown in Fig. 4(b). From this, it is observed that the applied gate voltage causes enough barrier reduction between the source and the channel, so that electrons easily flow from the source to the drain via the channel.

The high-k gate dielectric materials lead to better ON-

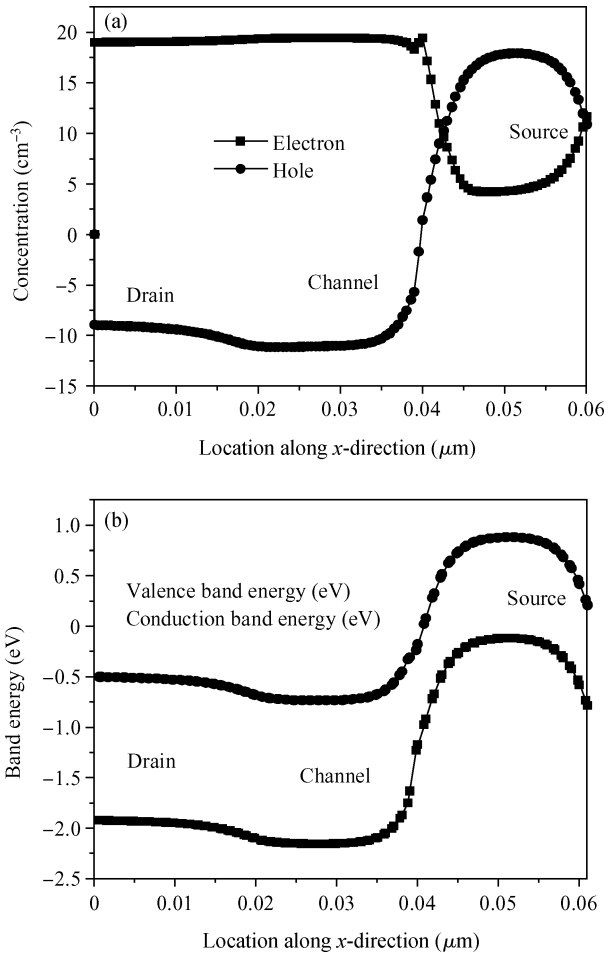

Fig. 4. (a) ON-state electron, hole concentration. (b) ON-state energy band diagram of H-JL-TFET.

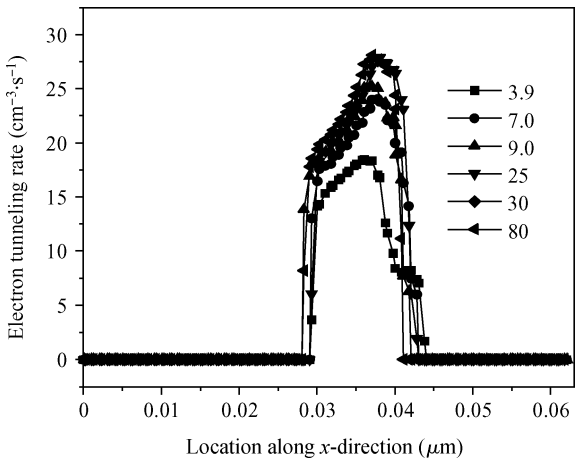

Fig. 5. Band-to-band electron tunneling rate versus relative permittivity with different gate materials at 300 K.

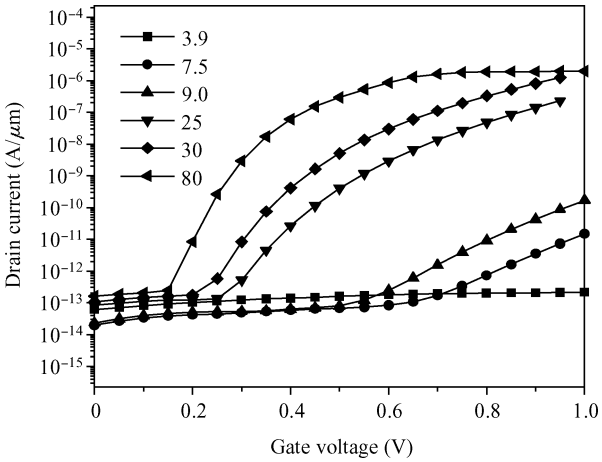

Fig. 6. Transfer characteristics of proposed simulated HJL-TFET with different gate dielectric materials at 300 K.

current characteristics of TFETs[24−27]. The careful choice of high-k dielectric material provides higher ON current (I_{ON}). Here in this work, the following dielectric material such as Si_3N_4 ($k = 7$), Al_2O_3 ($k = 9$), HfO_2 ($k = 25$), La_2O_3 ($k = 30$), TiO_2 ($k = 80$)[7, 20] and SiO_2 ($k = 3.9$) are used to observe the device performance. The physical thickness of the used gate dielectric material is 4 nm.

The ON-current (I_{ON}) of a tunnel FET depends on the width of the barrier between the channel and the highly doped source region. Since JL-TFETs are quantum mechanical devices (QMD) so current conduction in JL-TFETs is governed by band-to-band tunneling (BTBT) of electrons and is related to barrier width. Figure 5 displays the dependency of non-local band-to-band tunneling rate for the simulated device structure and it depends on gate voltage as well as gate dielectric materials. The BTBT rate of electrons is extracted from the simulated device structures for different gate dielectric materials. From Fig. 5, it is observed that high-k dielectric gate materials are suitable choices for better band-to-band tunneling (BTBT).

The ON-current (I_{ON}) and OFF-current of the simulated device are extracted at supply voltages of ($V_{G1} = -0.85$ V, $V_{GS} = 1.0$ V) and ($V_{G1} = -0.85$ V, $V_{GS} = 0.0$ V) respectively. The transfer characteristics for the proposed device with different gate dielectric materials are shown in Fig. 6. Figure 6 illustrates how the high-k gate influences the tunneling current of JL-TFET. From this figure, it is observed that the high-k dielectric material improves the ON-current (I_{ON}). Although high-k dielectric material enhances the transfer characteristics of the device, when it is directly put in contact with the silicon channel, it causes interface defects at the dielectric/semiconductor interface.

Investigation of I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio plays an important role in device characterization for digital circuit applications. The use of high-k gate materials helps in improving the I_{ON}, I_{ON}/I_{OFF} ratio and reducing the OFF-current. In this section we study the ON-current, I_{ON}/I_{OFF} ratio as well as OFF-current for the proposed simulated device. Figure 7 displays the variation of ON-current with different gate dielectric material. From this figure one can observe that high-k gate materials help in improving the ON-current. For validating the device performance, during investigation of device characteristics we use a large range of dielectric materials such as ($k \simeq$ 7.0, 9.0, 25, 30 and 80 respectively) and compare with SiO_2 ($k \simeq 3.9$). It is observed that there is slight variation in OFF-current (10^{-14}–10^{-13} A/μm) with a large range of used gate dielectric materials as shown in Fig. 8. It helps to optimize the OFF, i.e. leakage currents whereas good improvement in

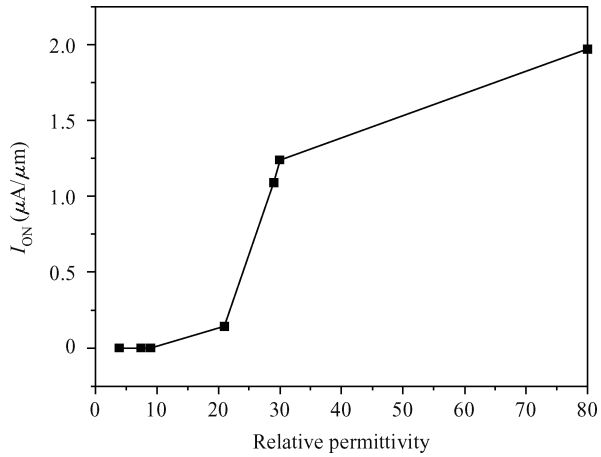

Fig. 7. Variation of ON-current (I_{ON}) with relative permittivity of gate material at 300 K.

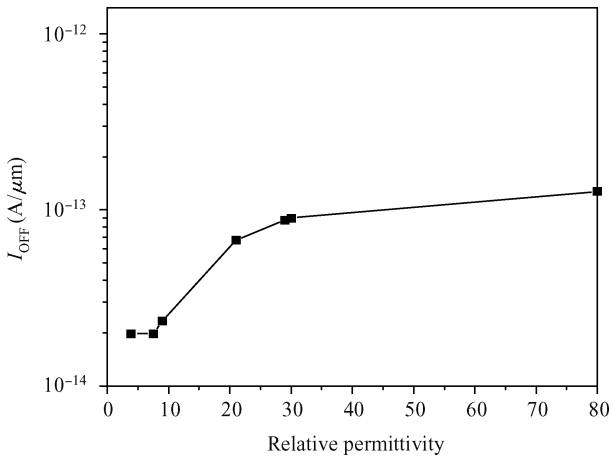

Fig. 8. I_{OFF} current versus relative permittivity of gate material at 300 K.

I_{ON}/I_{OFF} ratios; this is shown in Fig. 9.

Interestingly, the ON-current increases proportionally with increase in gate dielectric constant[20], which is observed from Fig. 7. Similarly, OFF-current also increases proportionally with high-k gate stack material, but there is very weak dependency when the dielectric constant of the gate is large as shown in Fig. 8. In our proposed device structure very small I_{OFF} ($\simeq 10^{-14}$–10^{-13} A/μm) currents are obtained for large values of dielectric constants of materials (i.e. 25, 30 and 80).

For conventional MOSFET, it is found that 60 mV/decade is the lowest possible subthreshold swing (SS) at room temperature[20, 28]. Figure 10 shows the variation of subthreshold slope versus gate dielectric materials. From this figure it is observed that our proposed device achieved SS of 41 mV/decade for TiO_2 ($k = 80$) at room temperature. This overcomes the limitations of traditional classical MOSFET. In conclusion it is clear that junctionless tunnel FETs are the best substitutes of MOSFETs for further development of low power, highly dense VLSI circuits[29, 30].

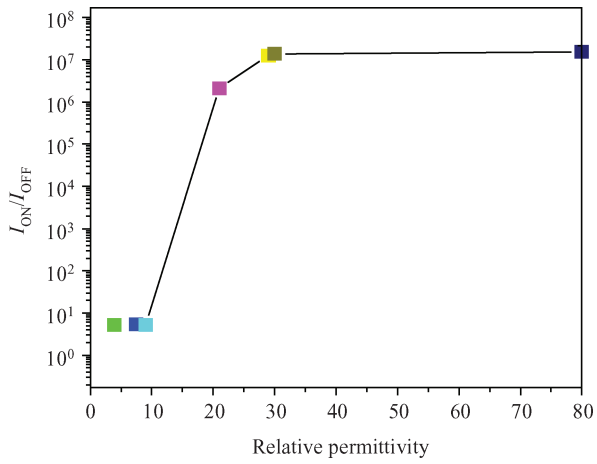

Fig. 9. Variation of I_{ON}/I_{OFF} ratios with various gate dielectric materials at 300 K.

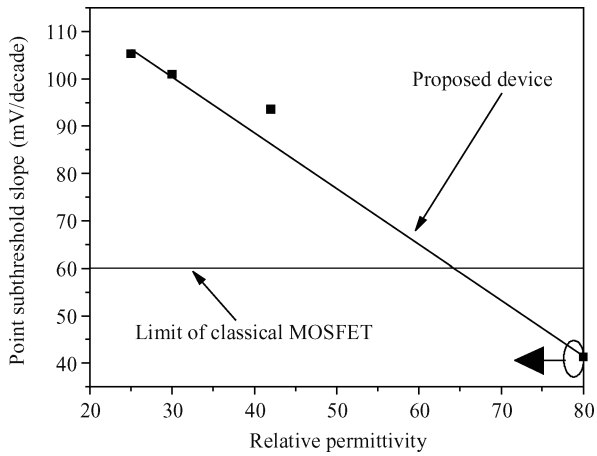

Fig. 10. Point subthreshold slope variation versus different gate dielectric materials at 300 K.

5. Conclusions

In this paper, a feasible and novel HJL-TFET is proposed and, by doing extensive simulations, its characteristics are thoroughly examined. The proposed device structure is extracted from a p–i–n diode and its fundamental working operation is based on band-to-band electron tunneling phenomena. During simulation we achieved steep subthreshold swing ($\simeq$ 41 mV/decade) with high on current ($\simeq 10^{-6}$ A/μm) and very low leakage current ($\simeq 10^{-13}$–10^{-14} A/μm). Thus HJL-TFET seems to be a strong candidate for replacement of MOSFET technology, particularly for low power applications for highly dense VLSI circuits.

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