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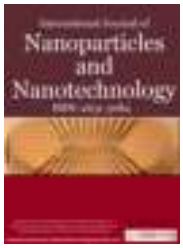
Suppression of Ambipolar Current and Analysis of RF Performance in Double Gate Tunneling Field Effect Transistors for Low-Power Applications



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Abstract

The present research letter is dedicated to a detailed analysis of a double-gate tunnel field-effect transistor (DG-TFET). The DG-TFET provides improved on-current (I_{ON}) than a conventional TFET via band-to-band (B2B) tunneling. However, DG-TFET is disadvantageous for low-power applications because of increased off-current (I_{OFF}) due to the large ambipolar current (I_{amb}). In this research work, a Si/GaAs/GaAs heterostructure DG-TFET is considered as research base for investigation of device performance. The electrical parameters of the DG-TFET device have been improved in comparison to the homostructure. The transfer (I-V) characteristics, capacitance - voltage (C-V) characteristic of homo structure Si/Si/Si and hetero structure Si/GaAs/GaAs, DG-TFET both structures is analysed comparatively. The C-V characteristics of DG-TFET have obtained using operating frequency of 1 MHz. The ambipolar current Iamb is suppressed by 5×10^8 order of magnitude in proposed Si/GaAs/GaAs hetero DG-TFET as compared to Si/Si/Si homo DG-TFET up to the applied drain voltage very low equal to VDS = 0.5 V without affecting on- state performance. The simulation result shows a very good I_{ON}/I_{OFF} ratio (10^{13}) and low subthreshold slope, SS (~36.52 mV/dec). The various electrical characteristics of homo and hetero DG-TFET such as on-current (I_{ON}), off - current (I_{OFF}), time delay (ι_d), transconductance (g_m) , and power delay product (PDP) have been improve in Si/GaAs/GaAs heterostructure DG-TFET and compared with Si/Si/Si homo DG-TFET. The advantageous results obtained for the proposed design show its usability in the field of digital and analog applications.

Keywords

Tunnel FET, Ambipolar current, Transconductance, C-V characteristics, RF performance, LPEs, PDP

Introduction

Progress in the development of low power electronics (LPEs) is reviewed by most suitable candidate named, tunneling field effect transistor popularly named Tunnel FET [1,2]. TFETs devices have emerged as a promising candidate for future low energy electronic circuit and system design. This device has attracted attention as a candidate for low-power applications because of its low subthreshold swing (SS) and negligible off-state current (I_{OFF}) compared with the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) [3-8]. The Tunnel FET is advocated as most appropriate candidate for low power applications

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but due their comparatively lower on-current (I_{ON}) must be improved to be compatible with future of VLSI circuit applications.

The Tunnel FET works by using modulated electric field by gate terminal, the width of tunneling barrier, instead of the height of a barrier that carriers must surmount via thermionic emission [9-12]. In TFET current transmission functions via tunneling transport mechanism, have weak temperature dependence and potential for subthreshold swing below the kT/q thermal limit of ~60 mV/decade at room temperature [13]. TFETs devices are not plagued by the similar short channel effects as MOSFETs. Although, the drain potential can affect the tunneling barrier at very short channel lengths, a reduction in supply voltage (V_{DD}) enabled by the steep subthreshold swing of a TFET can likely lessen the effect. Therefore, the TFET device structure potentially allows for scaling to shorter channel lengths prolonging Moore's Law, and these properties make TFETs a candidate for ultra-low power logic applications [13-15].

Owing to its distinct operation mechanism, namely band-to-band (B2B) tunneling, tunnel field effect transistors (TFETs) can overcome the subthreshold slope (SS) limitations of conventional MOSFETs and have thus attracted substantial attention for their use in low power applications. However, silicon (Si) based tunnel FETs always suffers from a low on-state current (I_{ON}) due large band gap (EG ~1.12eV) [16-19]. Therefore various approaches have been proposed by semiconductor device players to boost the band-to-band (B2B) tunneling current, such as using lower band-gap materials at the source or fabricating TFETs with a high-κ gate dielectric, with double-gate, with a high-κ spacer, and with a thin epitaxial tunnel layer (ETL) [20,21]. Although using, a low bandgap semiconductor materials in source terminal side, the tunnel region works to increase the tunnel current (I_{ON}), such devices subsequently have almost negligible off-sate current I_{OFF} (~10^{-18} A/µm). The high- κ gate dielectrics and high- κ spacers are used to enhance the electrostatics behavior of TFET devices [6,22-31].

In this work, the ambipolar current Iamb is suppressed by 5 × 10^8 order of magnitude in proposed Si/GaAs/GaAs hetero DG -TFET as compared to Si/Si/Si homo DG-TFET up to the applied drain voltage very low equal to VDS = 0.5 V without affecting on-state performance. The simulation result shows a very good $I_{ON}/_{IOFF}$ ratio (10^{13}) and low SS (~36.52 mV/dec). The various electrical characteristics of homo and hetero structured DG-TFET such as on-current (I_{ON}), off-current (I_{OFF}), time delay (ι_d), transconductance (g_m), and power delay product (PDP) have been improve for Si/GaAs/GaAs heterostructure DG-TFET and compared with Si/Si/Si homo DG-TFET.

Device Analysis Procedure (DAP) and setup

Figure 1 shows the 3D schematic view of homo and hetero structure double tunnel FET (DG-TFET), used in present research work. Figure 2a and Figure 2b shows, the Tony plot display using 2D mesh of double gate homo and heterostructure based on Si/Si/Si and Si/GaAs/GaAs semiconductor material for source, channel and drain region respectively.

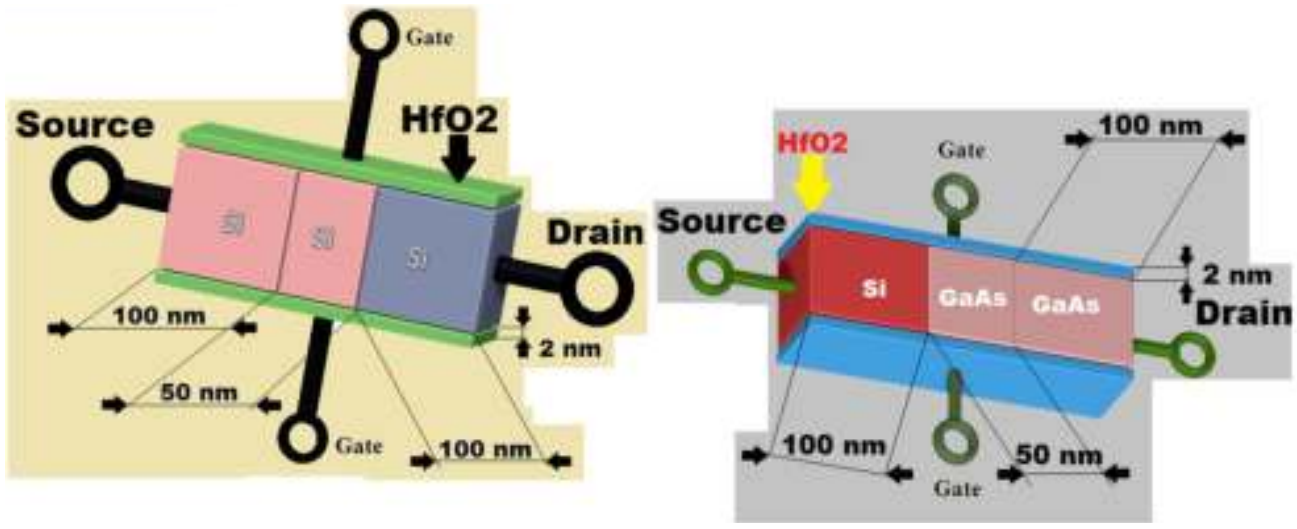

Figure 1: 3 D schematic homo and double tunnel FET.

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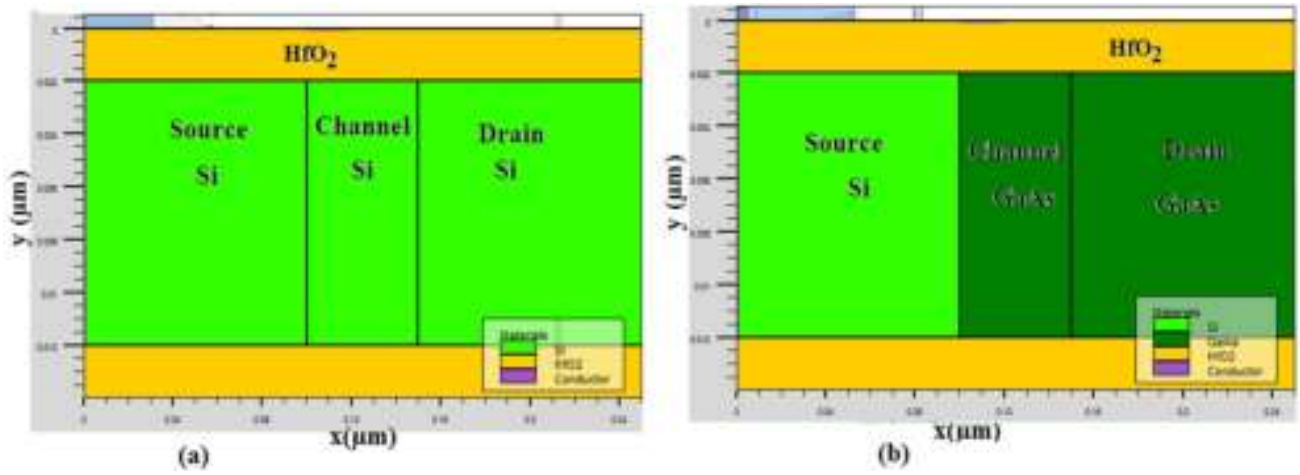

Figure 2: Tony plot display using 2D mesh of double gate (homostructure (a), heterostructure (b)).

Table 1: Design Parameters for Simulation double gate TFET.

Parameters	Nomenclature	Numerical value
ϕM	Work function (eV)	5.2
N_S	Doping levels for source (cm^{-3})	1.1×0^{20}
N_D	Doping level for Drain (cm^{-3})	5.1×0^{18}
N_C	Doping level for channel (cm^{-3})	10^{15}
t_{ox}	Gate oxide material thickness (nm)	2.0
L_t	Total length of the device (nm)	250.0
L_{ch}	Channel length (nm)	50.0
t_{Si}	Silicon film thickness (nm)	10.0
L_S/L_D	Source and drain lengths (nm)	100.0

The channel material with intrinsic carrier concentration $n_i = 1 \times 10^{15}$ cm^{-3}, channel thickness t_{Si} = 10 *nm* and channel length as in present research work. Figure 1b having same device dimension and is structurally same as silicon TFET except GaAs is used on drain side and channel side. All the remaining device parameters and dimensions of hetero gate (hetro DG) TFET and homo gate (homo DG) TFET are listed in the Table 1. The channel (L_{ch}) is 50 nm, source (L_s) and drain lengths (L_d) are 100 nm. The gate oxide material thickness (t_{ox}) is 2 nm and the silicon film thickness (t_{Si}) is 10 nm. The doping levels for source, channel, and drain regions are 1×10^{20}, 1×10^{15}, and 5×10^{18} cm^{-3}, respectively. The gate contact work function was set to be 5.2 eV.

All simulations of the DG-TFET, shown in Figure 1, Figure 2a and Figure 2b design have been carried out using Silvaco/ATLAS device simulator version 3.1.20.1.R in windows 7 operating system environment. The non-local BTBT model (BBT.NONLOCAL) was utilized. Fine meshing tunneling in the regions where BTBT mainly takes place were defined. Mesh size = 5×10^{-4} µm at interface source/channel and mesh size = 10^{-3} µm far of interface. The Newton's numerical method based on iteration was chosen to obtain a better convergence (CV). Further, to plot the figures of the high-frequency performance, a small-signal AC analysis was performed at a frequency of 1 MHz. The values adjusted to have the convergence for electron effective mass (m_e) and hole effective mass (m_h) used in the simulation are summarized on Table 2.

Current conduction in TFET is governed by band-to-band (B2B) tunneling between valence bands of source to conduction band of channel. This B2B tunneling is much more sensitive to material/device parameters such as energy bandgap (E_G), dielectric thickness (t_{ox}), gate-dielectric materials (κ), effective mass of charge carriers (m*) of tunnel devices, followed by Eq.1 . The position of the valence and conduction bands of the intrinsic part changes with the applied gate voltage. A conduction path by

Table 2: Listed parameters used in Si/Si/Si and Si/GaAs/GaAs DG-TFET.

Parameter	Materials	
	Si	GaAs
Energy Gap E_G (eV)	1.12	1.43
Effective electron mass m_e	0.12	0.067
Effective hole mass m_p	0.17	0.45
Mobility of electron μ_n ($cm^2.V^{-1}s^{-1}$)	8500	1345
Mobility of hole μ_p ($cm^2.V^{-1}s^{-1}$)	400	458

tunnel band-to-band (B2B) tunneling mechanism is then opened. The electrons can thus pass from the valance band (VB) of the p region to the conduction band (CB) of the intrinsic region and a tunnel current circulates in the device (the transistor is then in the on-state). The on-current ION of a DG-TFET, in the tunnel band-to-band (B2B) tunneling mechanism is proportional to the transmission probability T (E) of the electrons or holes by tunnel effect, which is written by mathematical expression 1.

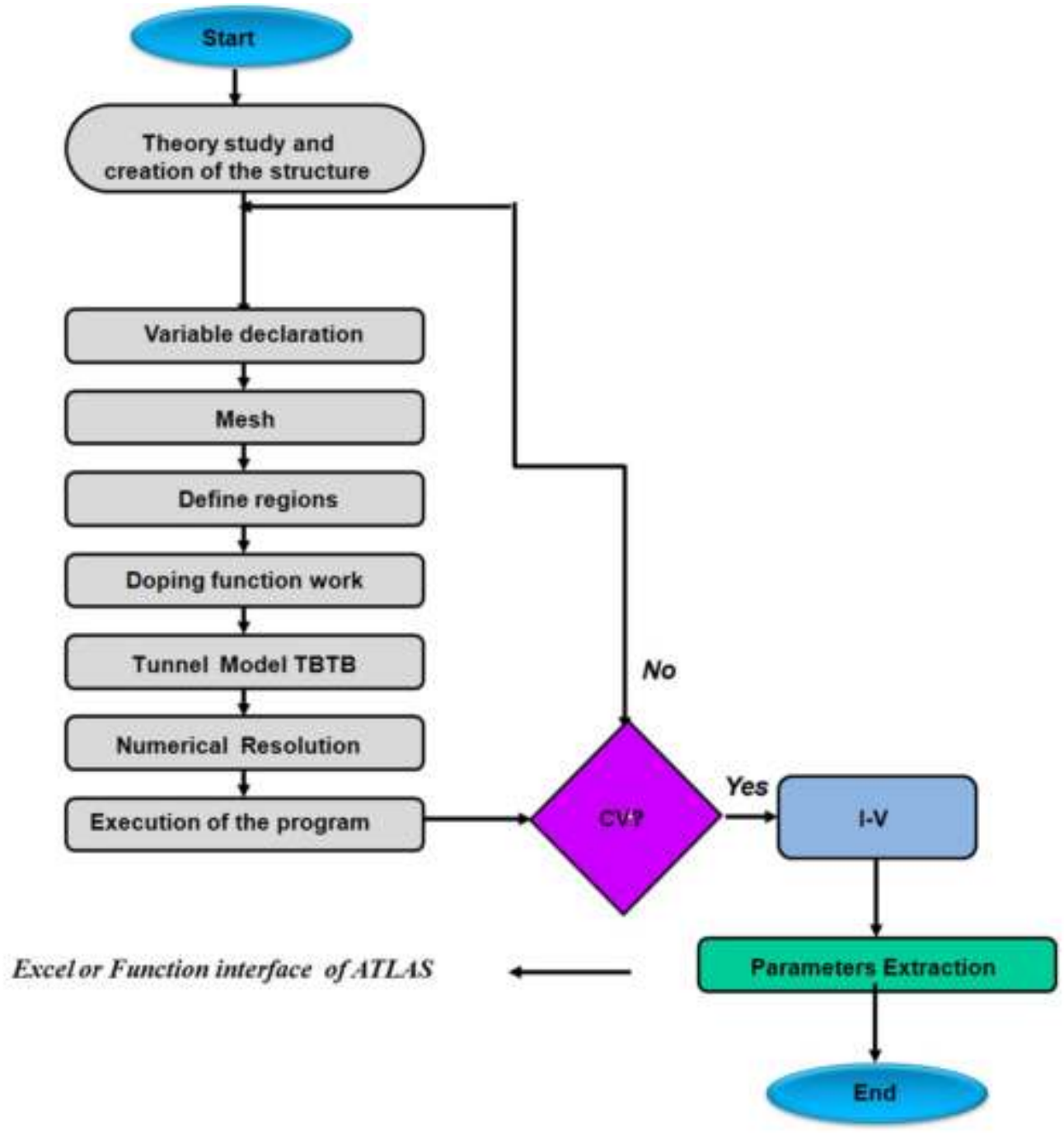

Figure 3: Atlas resolution algorithm of double gate TFET.

$$T(E) \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar\left(E_g + \Delta\phi\right)} \right) \quad (1)$$

The tunneling distance (λ) is determined by following mathematical expression (2). In Eq.1, m* is the effective mass and EG, is the band gap. The symbol λ denote, the tunneling distance between the source and the channel, ΔΦ denotes the band energy difference between the conduction band of source and valence band of the channel. The symbol ħ, e denotes reduced Planck's constant and electronic charge respectively. While, the symbol t_{ox} and t_{si} has been for physical oxide thickness, and semiconductor channel thickness respectively. The symbol ε_{ox} and ε_{si} denote dielectric constants for oxide and silicon respectively [7].

$$\lambda = \left(\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox}\ t_{Si}} \right)\Delta\phi \quad (2)$$

In this work, simulation is done using SILVACO

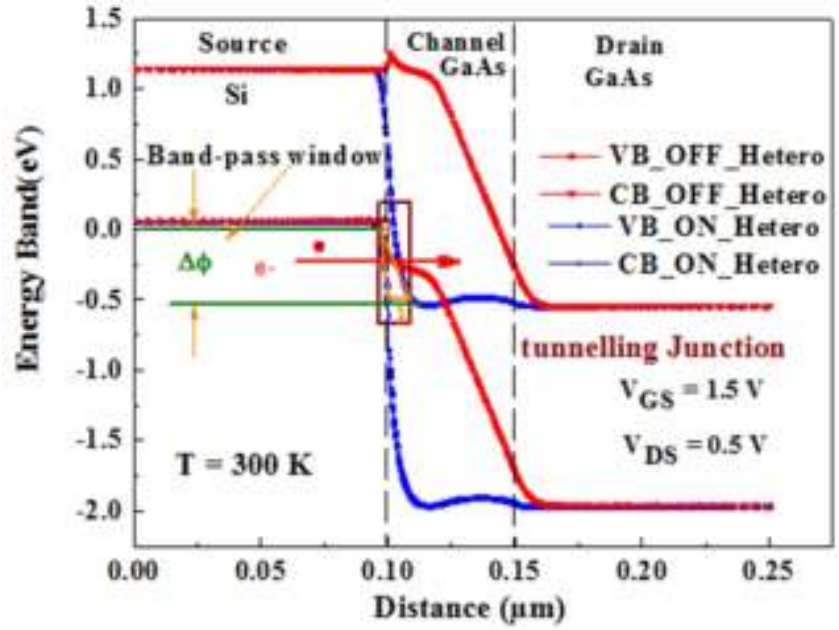

Figure 4: Energy band-diagram (OFF-State and ON-State) for hetero structure DG-TFET.

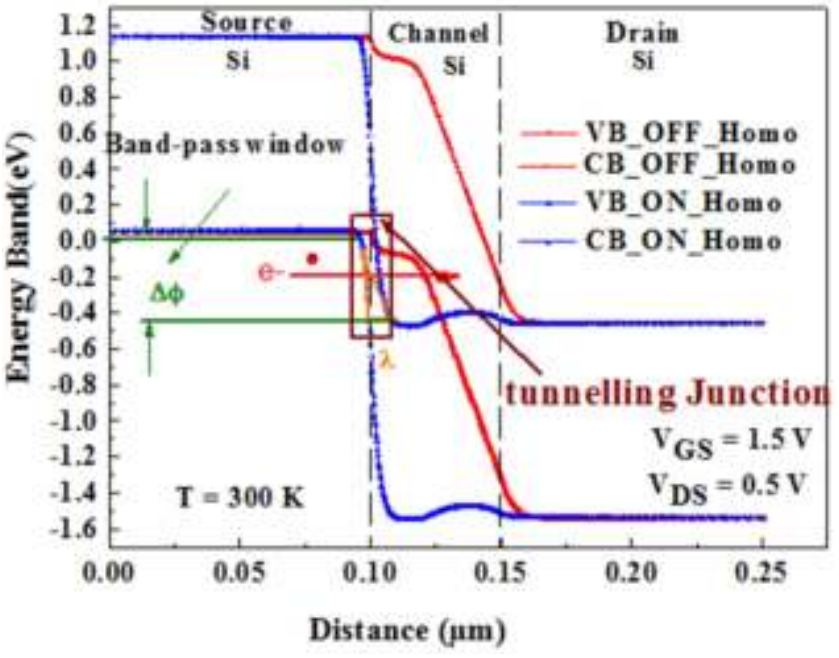

Figure 5: Energy band-diagram (OFF-State and ON-State) for homo DG-TFET.

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ATLAS. In the simulation non-local B2B Tunneling model is considered for the band to band tunneling of charge carrier between source and channel. Due to high doping of source band gap narrowing (BGN) model is also included, because effective bandgap directly influence the tunneling current. The Shockley-Read-Hall (SRH) recombination model have been due to the presence of high impurity atom in the channel and Fermi Dirac statistics for calculating intrinsic carrier concentration. For more accurate current calculation Schenk's Trap assisted Tunneling (TAT), drift-diffusion current transport model, and Quantum Confinement (QC) models are also included. Figure 3 represent the flow chart for present research work.

Figure 4 and Figure 5 show the energy band diagram of DG -TFET. As shown in Figure 4 and Figure 5, when VGS = 0.0 V, the device is in off-state with large tunnel barrier width λ, and therefore the charge carrier, electrons do not have enough energy to move from the valance band of the source to the conduction band of the channel. On application of sufficiently high gate voltage (i.e. V_{GS} = 1.5 V and V_{DS} = 0.5 V), the width of tunneling barrier λ is reduced significantly and the device switches to on-state.

When the device switched from, the off-state to the on-state, an increase in the electric field is observed [5]. It has been observed that the tunnel barrier, λ decreases and there is a shift of the conduction band downwards. Thus, the gradual enhancement of the gate bias, VGS degrades the barrier width and causes an increased tunneling of carriers, indicated in Figure 4 and Figure 5. The simulation results indicate that, hetero double gate TFET, having smaller tunneling width λ. For hetero and homo structured double gate TFET, tunneling with λ, 0.05 μm and 0.056 μm is obtained during simulation respectively.

Result and Discussion

The tunneling barrier width λ has been reduced in case of heterostructure TFET due to lattice mismatch between Si and GaAs semiconductors at channel interface. This causes increment in tunneling current due induced stain in tunneling region. This results, the higher on-state current (I_{ON}) as shown in Figure 6.

Figure 6 shows the transfer characteristic of DG -TFET shown in Figure 1. It has been observed from Figure 6 the comparision of transfer characteristics of homo and hetero structure DG -TFET.

From Figure 6 one can observed, the drain current, IDS increased rapidly with the drain voltage,

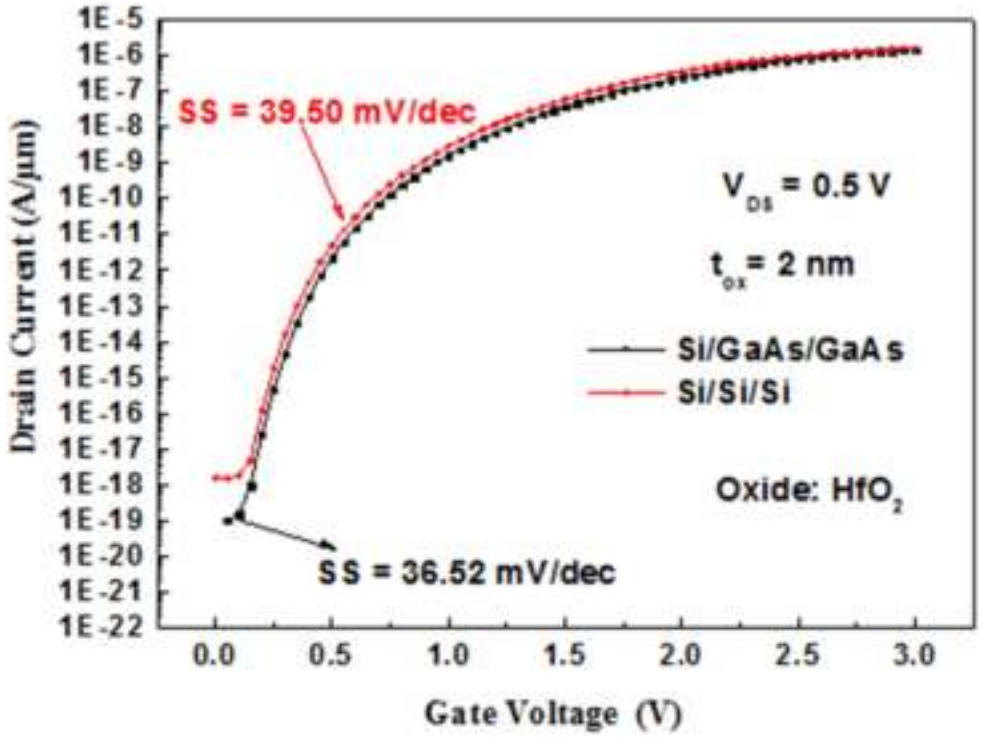

Figure 6: Comparision of transfer characteristics of homo and hetero structure double gate tunnel FET.

VDS equal to 0.5 V the output current of hetero was higher than that the homostructure of the DG-TFET. Table 3, lists of the computed electrical parameters of the DG -TFET. As shown in Table 3, various electrical parameters such as on-state (ION), off-state (I_{OFF}), subthreshold slope (SS) and I_{ON}/I_{OFF} ratio have improved. While ambipolarity current I_{amb} (A/µm) has been reduced by order of ~10^8 times.

Figure 7 shows, the comparision of ambipolar property of homo and hetero structure DG-TFET. The result shows that, suppress the ambipolar current (I_{amb}) without deteriorating analog, and transient performance. From Figure 7, It has been observed, with the help of 2-D. TCAD simulation that, the ambipolar current, I_{amb} is suppressed by 5.10^8 order of magnitude in proposed Si/GaAs/GaAs hetero DGTFET as compared to Si/Si/Si homo DG -TFET up to the applied gate voltage of V_{GS} = -3.0 V the step of gate voltage was taken equal to 0.5 V. The computed electrical parameters of the both structures are listed in Table 3.

Table 3: Lists of the computed electrical parameters of the DG-TFET.

	Dielectric HfO_2	
Electrical Parameter	**Homo_DGTFET -TFET**	**Hetero_DG -TFET**
I_{ON} (A/µm)	4×10^{-6}	5×10^{-6}
I_{OFF} (A/µm)	10^{-18}	1.1×0^{-19}
I_{ON}/I_{OFF}	4×10^{12}	5×10^{13}
S (mV/dec)	39, 50	36, 52
I_{amb} (A/µm)	5×10^{-11}	10^{-19}

The transconductance g_m represents amplification ability of device and it is defined as the slope of the transfer characteristic was used to evaluate the simulation performance of the device, the value of g_m can be calculated by mathematical expression (3):

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad (3)$$

As shown in Figure 8, the transconductance g_m for both structures i. e. hetero and homo structures increase rapidly as external applied gate voltage V_{GS} increases. The maximum g_m value of the hetero DG-TFET heterostructure is 1.6 µS/µm and the maximum g_m value of the homo DG-TFET homostructure is 1.4 µS/µm. The larger gm of hetero is larger than homostructure because the barrier width of tunneling junction decreases; the tunneling electrons increase (shown in energy band diagram Figure 4 and Figure 5). The transconductance

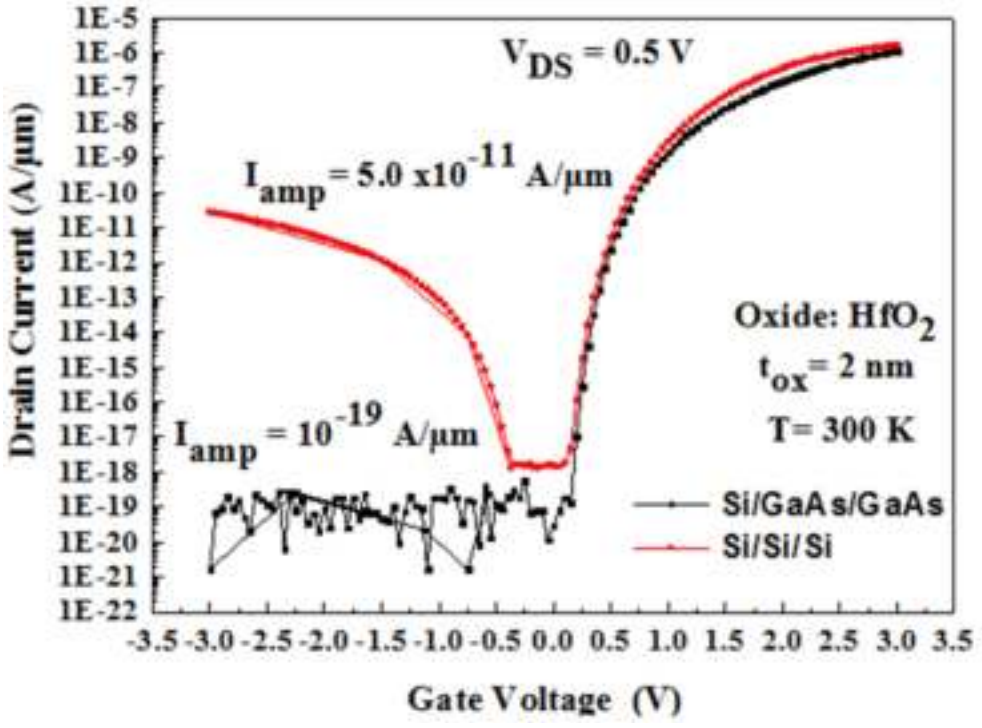

Figure 7: Comparision of ambipolar property of homo and heterostructure double gate tunnel FET.

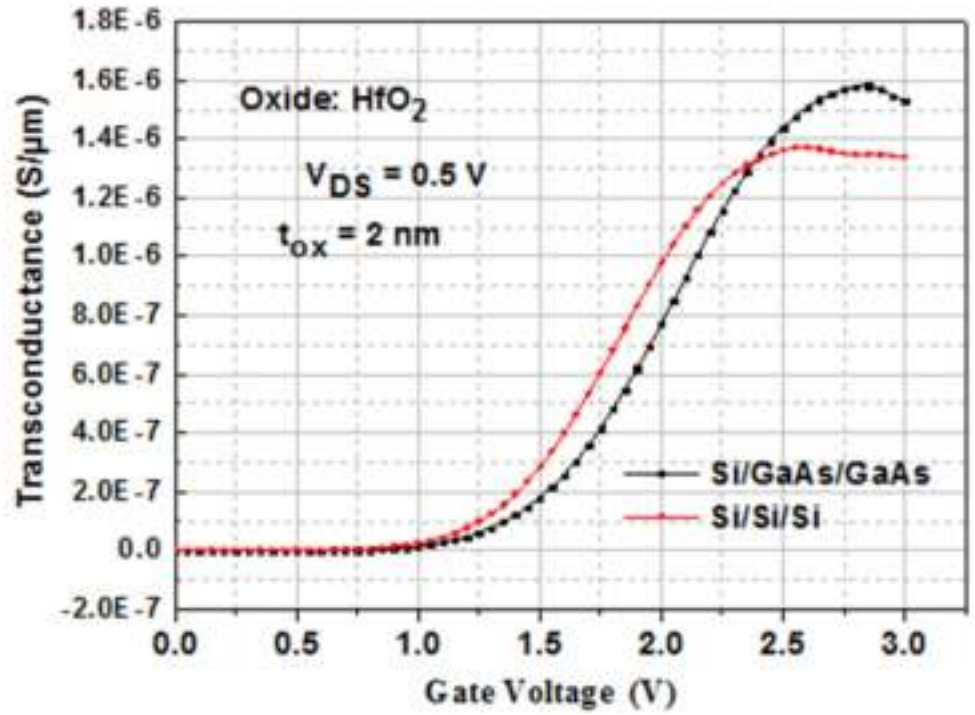

Figure 8: Comparision of transconductance of homo and heterostructure double gate tunnel FET.

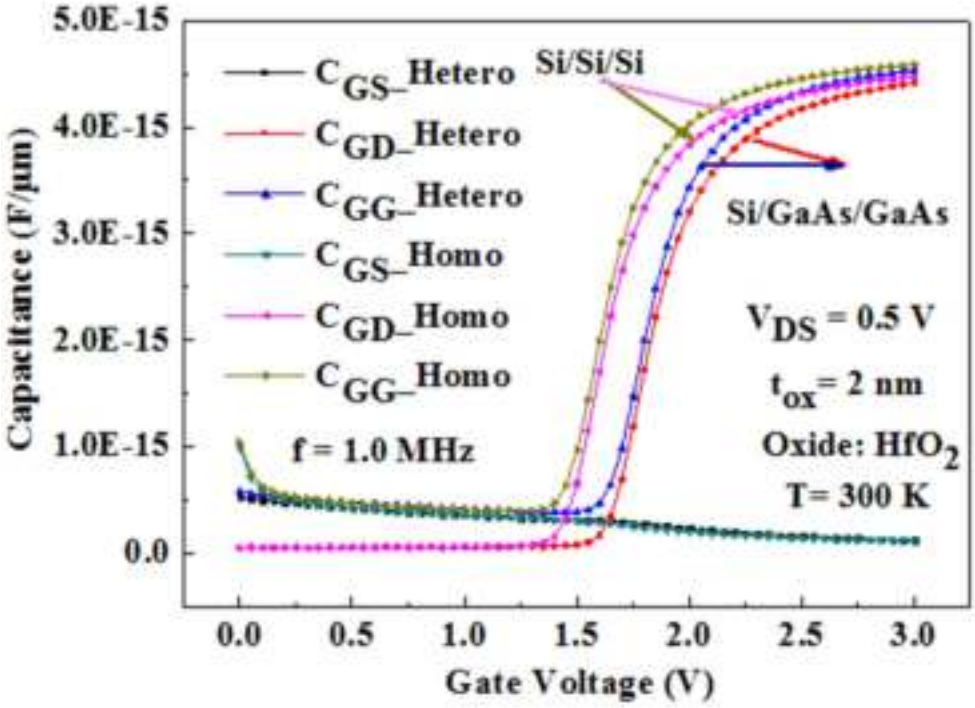

Figure 9: Comparision of C-V characteristics of homo and heterostructure double gate tunnel FET.

(g_m) of a device depends on the value of drain current IDS. So, the drain current is higher for Si/GaAs/GaAs DG - TFET compared to DG-TFET Si/Si/Si, due to the increase of tunneling volume in the channel.

Figure 9 shows the capacitance of different structure, as shown, an increase in the capacitance from bottom to top at the threshold voltage, The Gate-Gate capacitance is mainly composed of two capacitances Gate-Drain (Cgd) and Gate-Source (Cgs), Gate-Source capacitance is lower because

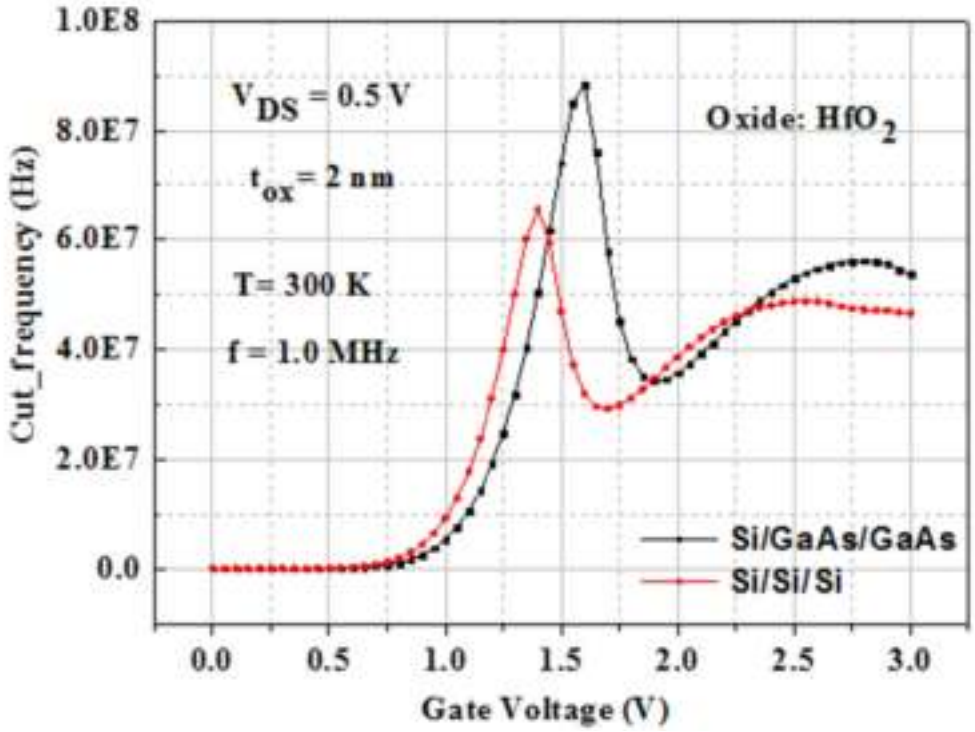

Figure 10: Comparision of cut-off frequency of homo and heterostructure double gate tunnel FET.

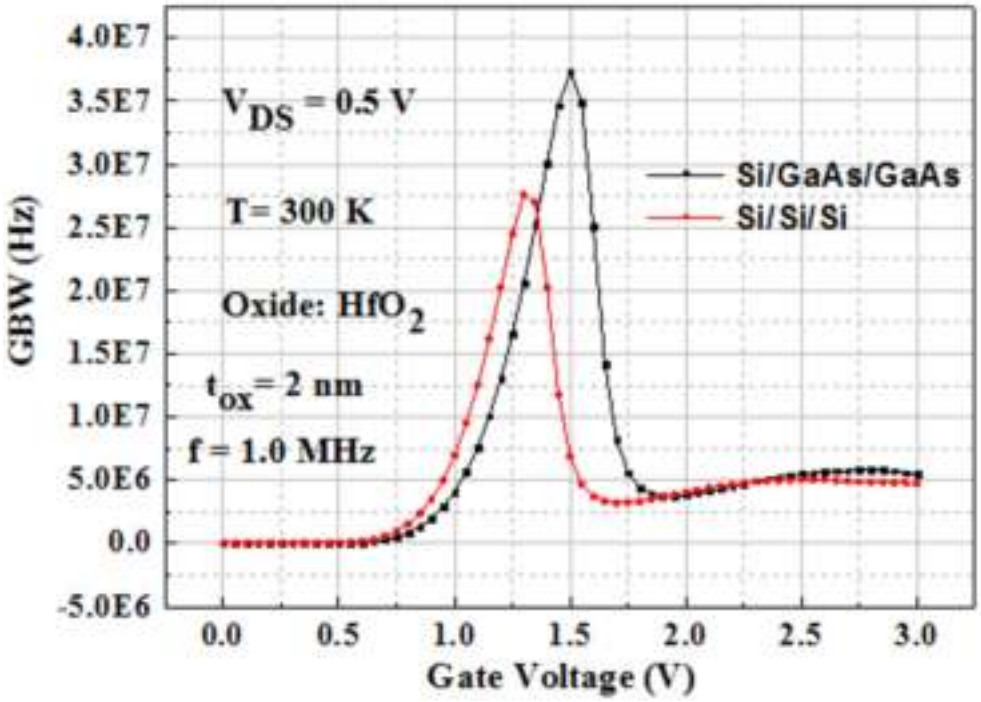

Figure 11: Comparision of gain band width (GBW) of homo and heterostructure double gate tunnel FET.

the presence of the tunnel effect, the Gate-Drain capacitance is a dominant capacitance due to the accumulation of the electrons of the Canal-Source and collected by the Drain region.

As an important indicator, the cut-off frequency is used to evaluate the frequency characteristics of electronic devices. It can be obtained by the ratio of g_m to Cgg, with following relation, equation 4.

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} = \frac{g_m}{2\pi C_{gg}} \quad (4)$$

In Figure 10, as the gate voltage increases, the the cut-off frequency f_T increases to reach its maximum, then with increasing Cgg it goes down, when the gate voltage V_{GS} reaches 2.0 V the cut off frequency becomes constant. This is because the on-state current and gm value increase with the electronic B2B tunneling, the cut-off frequency of Hetero is much larger than that of homo, which can be explained by the smaller Cgg of hetero structure DG-TFET and the larger of the gm value. Table 4 resume values of f_T for both structures. This observation is verified in Figure 11 that show gain band width versus gate voltage V_{GS}. It has been observed that, the simulation results predicts decreased gate capacitance with decreased operating voltage V_{GS}, as depicted in Figure 9 which gives the variation of the gate capacitance with V_{GS}. It is should be noted that, the capacitances of TFET is bias-dependent. That is to say, the decrement rate of the gate capacitance with frequency is bias-dependent.

The gain bandwidth product (GBW) is another important indicator in the analysis of frequency characteristics, which can be calculated by the equation 5.

$$GWB = \frac{g_m}{2\pi 10 Cgd} \quad (5)$$

Another important performance parameter for RF analysis is transit time given by expression (6). According to this mathematical expression, time is inversely proportional to the cut-off frequency. If the cut-off frequency increases the transition time decreases. As a result, the speed of the heterojunction DG-TFET structure is better than that of homojunction DG-TFET, estimated cut-off frequency is smaller. Figure 12 shows the delay time versus gate applied gate voltage. From Figure 12, it can be observed that, the simulation results predicts increased delay time with increased operation gate voltage VGS. It is should be noted that the delay time is bias-dependent.

That is to say, the decrement rate of the gate voltage V_{GS} with hetero gate double DG-TFET with smaller delay time than homo structure DG-TFET. The delay time of V_{GS} = 2.0 V decreases rapidly.

$$\tau_d = \frac{1}{2\pi f_T} \quad (6)$$

It can be observed that, the simulation results predicts increased power delay product (PDP) with

Table 4: Cut off frequency values for double gate TFET.

High-k gate	Cut-off frequency T	
Dielectric HfO_2	V_{DS} = 0.5 V	V_{DS} = 2 V
Hetero structure	~ 0.1 GHz	3 GHz
Homo structure	~ 65 MHz	1.4 GHz

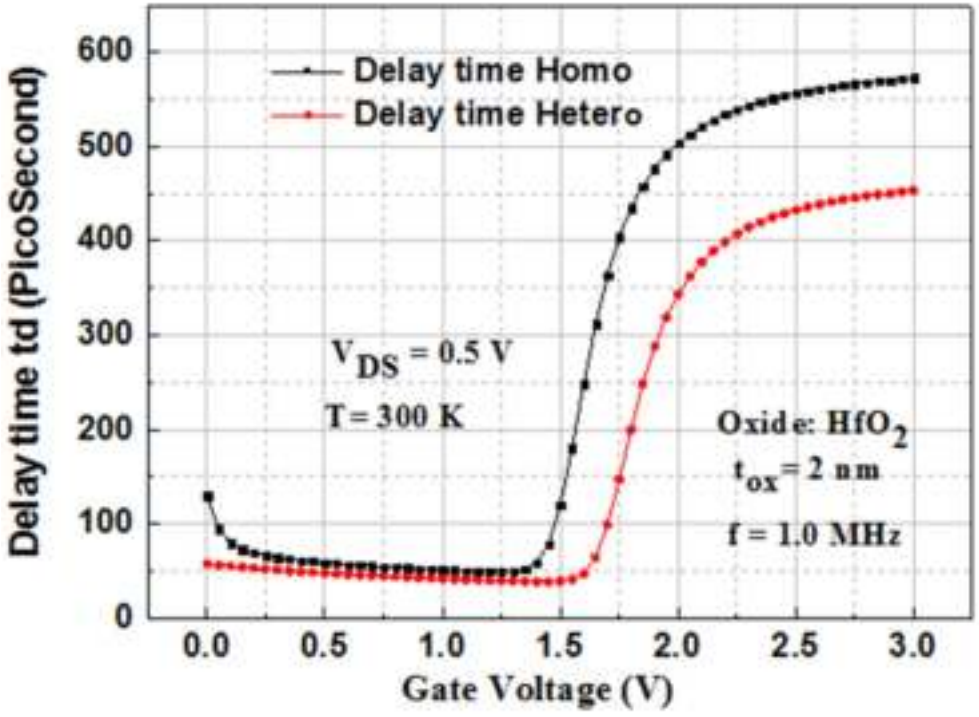

Figure 12: Comparision of delay time of homo and heterostructure double gate tunnel FET.

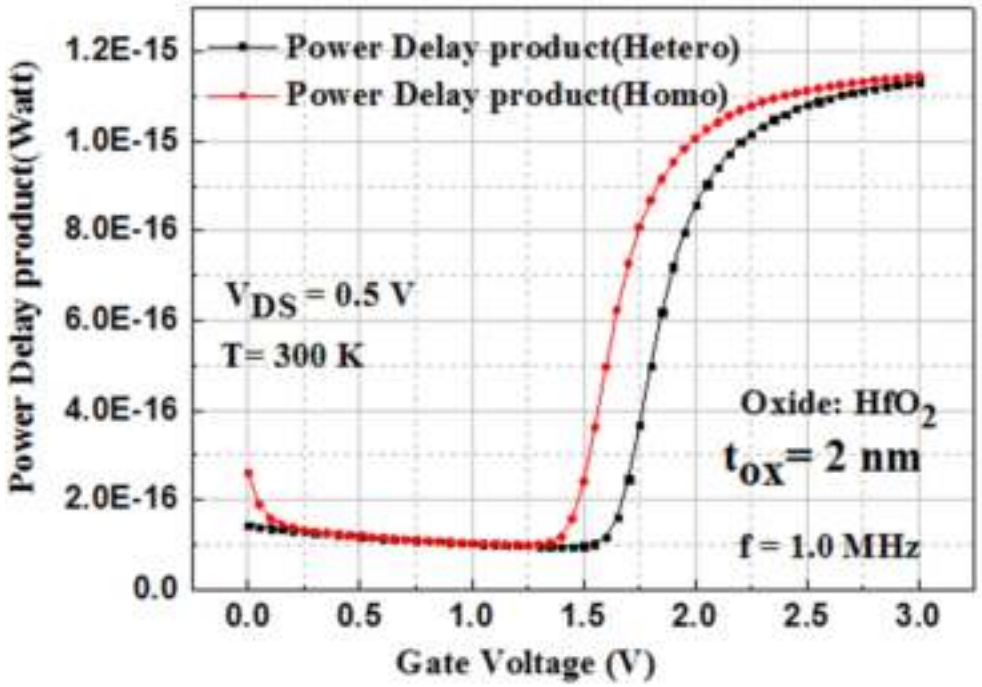

Figure 13: Comparision of Power delay product (PDP) of homo and heterostructure double gate tunnel FET.

increased operation gate voltage V_{GS}, as depicted in Figure 13, which gives the variation of the power delay product (PDP) with gate applied gate voltage V_{GS} . It is should be noted that, the power delay product is bias-dependent. That is to say, the decrement rate of the gate voltage with hetero gate double gate with smaller power delay product (PDP). The delay time of V_{GS} = 2.0 V decreases rapidly.

Conclusion

In the present work, 2-D TCAD Silvaco simulations are used to study the impact of heterojunction on the DC, analog and PDP. In the adopted double gate TFET design achieved on-state current of 5 × 10^{-6} A/µm, I_{OFF} of 1 × 10^{-13} A/µm , SS of ~ 36 mV/decade, and maximum cut off frequency in the game of the RF also a very weak power delay product about of 1.1 × 10^{-15} Watt. Also the value of delay time t_d reach is obtained in picoseconds range (~ 600 Picoseconds). By using, heterojunction DG-TFET structure, it have observed the suppression of the ambipolar current I_{amb} ~ 10^{8} A/µm times. The advantageous results obtained for the proposed design show its usability in the field of digital and analog applications. These results are crucial for enabling a full and accurate assessment of TFETs through circuit predictions.

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