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A Review Report on Ballistic Transport and Self Heating Effect (SHE) in Nanoscale Strained –Silicon MOSFETS

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***Abstract*- As MOS Transistors channel length continues to scale beyond 90nm, classical drift-diffusion model for carrier transport of such type of devices is not valid. For these dimensions of Transistors Quasi- Ballistic/ Ballistic transport phenomena occur and a new mobility model is required to predict electrical behavior of these devices perfectly. Self-heating is also one the importance critical problem for Nanoscale devices. In this article we re -examine the "Ballistic mobility" and "self-heating" for Nanoscale strained-silicon MOSFETs.**

***Keyterms*- Ballistic Transport, MOSFET, Strained – Silicon, Self Heating Effect (SHE), Bulk MOSFET**

I. INTRODUCTION

Geometric scaling of MOSFET channel length and to enhance drive current and speed has become and extremely expensive and complex task. Strain engineering is an alternative approach to improve the clock frequency, by enhancing mobility of the electrons and holes in the channel of Nanoscale MOSFETs [1].The influence of strain on the intrinsic mobility of Si was first investigated in early 1950's. While this effect was not exploited initially, the idea was received at MIT in the early 1990's. In 1992 it was first demonstrated that n-channel MOSFETs on a strained Si substrate, exhibit a 70% higher effective mobility (μ_{eff}) than those of unstrained substrates. Even though since semiconductor industry has adopted several different technologies to introduce strain in the Si channel of MOSFETs [2].Recent works have shown that the mobility of electrons can be increased between 15-25% compared to the conventional transistor by using a strained thin epitaxial Si layer grown on a relaxed $Si_{1-x}Ge_x$ substrate [3].

Generally, there are two approaches for introducing strain in MOSFETs can be identified as global, where stress is introduced across the entire substrate, and local approach, where stress is introduced into the device by means of shallow- trench- isolation, epitaxial layers and/or highly stressed nitride capping Layers[2,4]. As shown in Fig-1 and Fig-2.

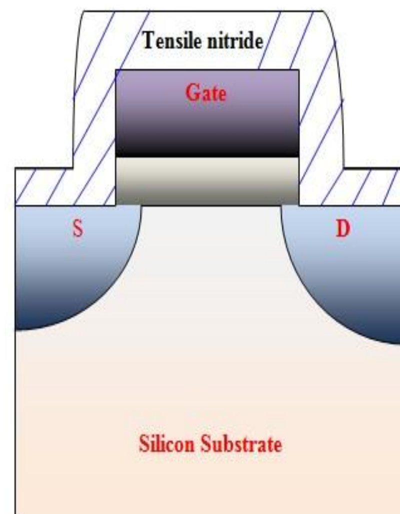

Fig .1: Schematic diagram of Uniaxial- Strained Silicon MOSFET.

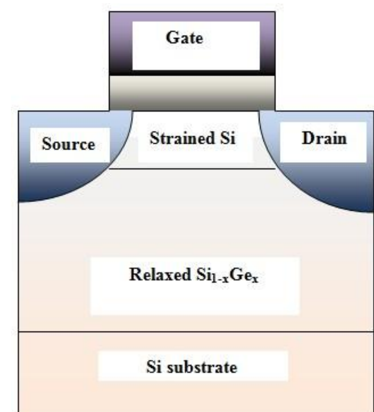

Fig.2: Schematic diagram of Biaxial Strained Silicon MOSFET.

II. STRAINED ON BAND-STRUCTURE

Strain technique has been gaining attention due to their higher mobility and compatibility with conventional bulk – silicon CMOS technology.

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A thin layer of strained silicon grown on top of a relaxed silicon germanium substrate as shown in Fig-3 exhibits a type || band offset. There are band offsets in both the conduction and the valance bands. The conduction band and valance offset causes the confinement of electrons and holes and advantageous in nMOS and pMOS respectively [3,4].The conduction and valance offset set is calculated by following Equation-1 and 2 respectively [5, 6, 7, 8].

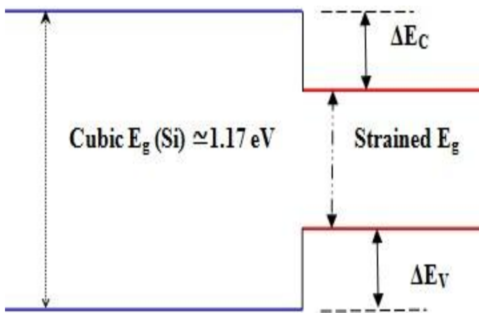

Fig.3: Illustration of band-structure in strained silicon MOSEFTs.

$$Conduction\ band\ offset,$$

$$\Delta E_c = 0.63 \quad (1)$$

and $Valance\ band\ offset,$

$$\Delta E_v = x(0.74 - 0.53x) \quad (2)$$

and band gap in strained-silicon layer is effectively narrower according to [9] Equation-3

$$\Delta E_g(sS) = E_g(Si) - E_g(sS) = 0.4x\ eV \quad (3)$$

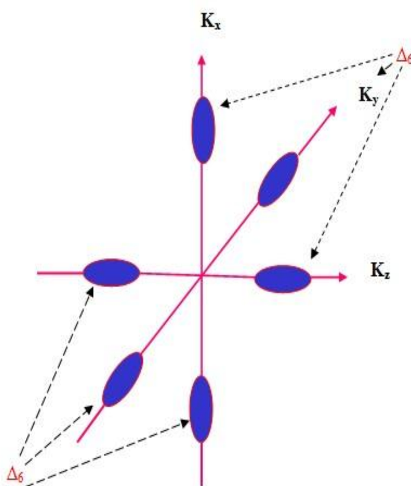

Fig.4: Band Structure of Unstrained Silicon.

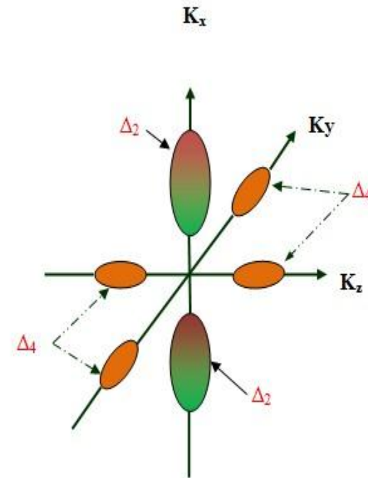

Fig.5: Energy band splitting due to applied strain in conduction band.

One of the interesting issues related to strained- Si transistors is the modulation of the sub-band structure due to stress as shown in Figure-5. In bulk Si, the conduction band consists of six equal valleys (Δ_6) with same energy. The stress longitudinal to<110> direction (channel direction) could remove the degeneracy between the four in-plane valleys (Δ_4) and the two out-of- plane valleys(Δ_2) due to splitting[3] as shown in Fig-5,in addition, change induced in the conduction band curvature significantly reduced electron effective masses[5,10] as shown in Fig.6

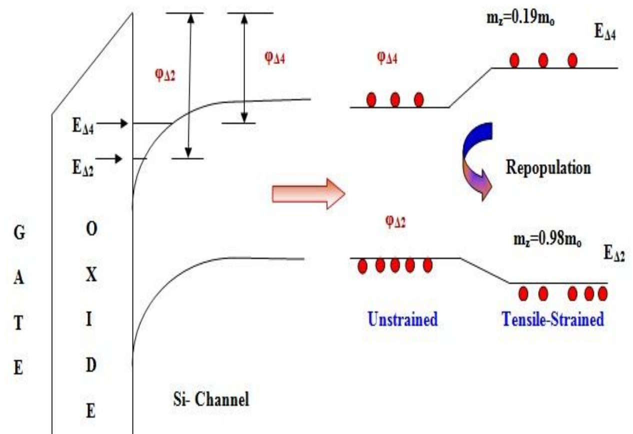

Fig.6: Illustration of applied stress in band structure of Conduction band in NMOSFET.

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III. CARRIER TRANSPORT IN ULTRA-SCALED MOSFETS

Recently, Intel announced plans of 15 nm Si CMOS technology for Intel Atom processors based System-on-Chip (SOCs) [10]. Since the covalent diameters of a Si atom are 0.234nm, there will be only 64 Si atoms under the gate of such a device. In this regime; conventional model of electron mobility becomes invalid [10, 11].

In the ballistic or quasi- ballistic regimes, the conventional device equations based on the drift-diffusion theory are not valid, and consequently a theory of ballistic transport is need. Natori first developed this theory for silicon MOSFETs, and it has extended to a general ballistic model. Recently, Shur has also introduced the concept of "ballistic mobility" in order to capture ballistic effects in the short channel High Electron Mobility (HMET) while retaining drift- diffusion formalism [12].

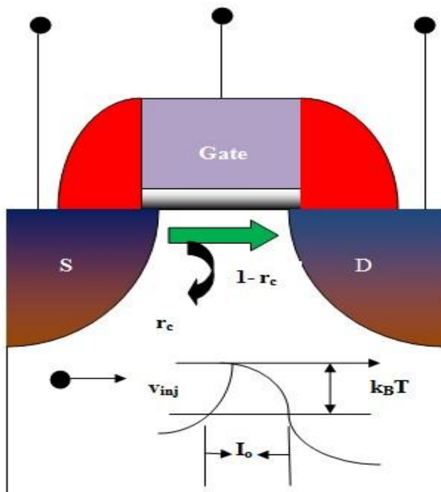

Fig.7. Illustration of ballistic transport phenomena in ultra-scaled MOS Transistors.

In order to realize high speed logic CMOS devices, it is necessary to increase the carrier mobility for device gate length down to the 90-nm and beyond. The drain current for a device in the ballistic regime is governed by [13, 14, 15 19]

$$I_{D,Sat} = WC_{eff}V_{inj}B_{sat}(V_G - V_{th}) \qquad (4)$$

Where V_{inj} and B_{sat} are the source injection velocity and the ballistic efficiency respectively. The coefficient of B_{sat} is[16,19]

$$B_{sat} = \frac{1-rc}{1+r_c} \qquad (5)$$

The Reflection coefficient r_c, is expressed as

$$r_C = \frac{1}{1+\frac{\lambda_O}{L_{kBT}}} \qquad (6)$$

The carriers with the injection velocity, V_{inj}, are injected from the thermal source, travelling to drain side, while those which cannot surmount the channel barrier will reflect to the source region. This reduces the drain current. As a consequence we need large B_{sat} for better performance means lower reflection. In MOSFETs, carriers are injected from source into barrier whose channel barrier is modulated by the gate voltage. The source-channel barrier becomes more important in short channel devices and will ultimately limit the drain current (I_{DS}). From the scattering theory, the two fundamental transport parameters, the backscattering (ballistic efficiency) and the carrier injection velocity from source, are strongly dependent on the strain technique [19].

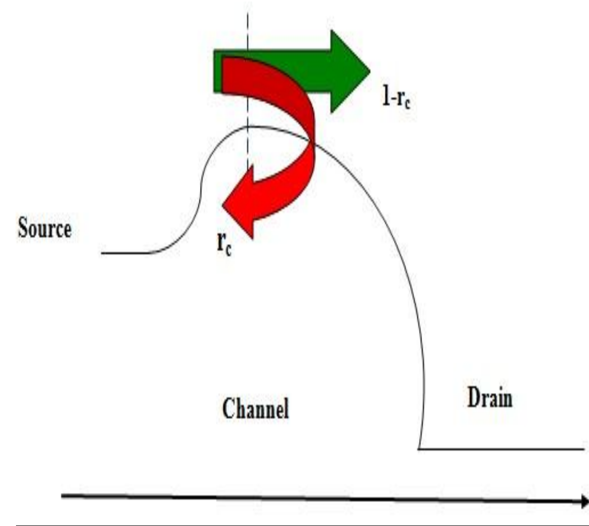

Fig.8: A schematic diagram of Backscattering in Nanoscale MOS Transistor. Channel backscattering takes place mainly at the source end in which potential drop is less than kT/q.

The generalized form for backscattering coefficient is defined by following relation [21]

$$r_c = \frac{\lambda^{-1}}{\frac{1}{2}\left(\frac{q|E|}{kT}\right)*\left(1+\coth\left(\frac{x}{2}*\frac{q|E|}{kT}\right)\right)+\lambda^{-1}} \qquad (6)$$

Where q is the electronic charge, k is the Boltzmann constant, T is lattice temperature. E is the electric field, and λ is the mean free path. Now substituting $x = L_c(Channel\ lenght)$ and $E\ by\ V_{DS}/L_c$ [16,21]

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$$r_c = \frac{L_{kT}}{\lambda_0 + L_{k_BT}} \quad (7)$$

Where L_{k_BT} (also called the "k_BT layer") represents the critical distance over which the scattering events modify the current, and its value depends on the drain-to-source voltage as defined as

$$L_{K_BT} = L_c\left(\frac{kT}{q}V_{DS}\right) \quad (8)$$

Mean free path directly obtained as [16]

$$\lambda_0 = \frac{2}{v_{TH}}\frac{kT}{q}\mu_o \quad (9)$$

Where v_{TH} is the thermal velocity, which can be expressed as $v_{TH} = \sqrt{2kT/\pi m^*}$, $1.2x10^7 cm/s$ for electrons and $7x10^6$cm/s for holes and μ_o is the effective low field mobility. Even though the free path becomes shorter as the channel length decreases, number of scattering in the channel also decreases due to the less number of scattering centers/atoms in channel. Interestingly, backscattering coefficient decreases as rapid scaling down of the device channel length as shown in Fig.9

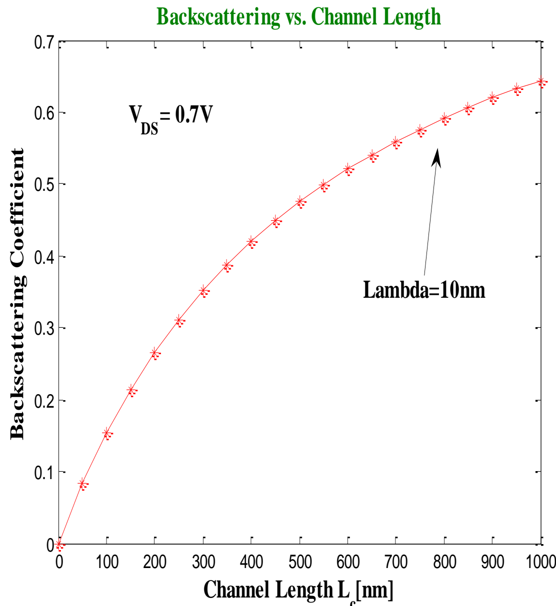

Fig.9: Variation of Backscattering vs. Channel length in Nanoscale MOSFETs

IV. Ballistic Mobility Model For Nanoscale Strained Silicon MOSFETs

Shur introduced the new concept of ballistic mobility μ_B and provided an expression valid for nondegenerate conditions. The motivation is to retain the form of the traditional FET model in quasi-ballistic regime, where mobility loses its physical basis. In quasi- ballistic regime, the mobility used in the conventional device equations is replaced by an effective mobility $\mu_{eff,}$ which is calculated by Mathiessens's rule as [12,17], by Equation-

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_B} + \frac{1}{\mu_o} \quad (10)$$

In Equation -10, μ_o is physical mobility in long channel device, where scattering - dominated

$$\mu_o = \left(\frac{q}{k_BT}\right)D_n \quad (11)$$

Equation-12, define nonphysical ballistics mobility

$$\mu_B = \left(\frac{qL_c}{\pi m^* v_{TH}}\right) \quad (12)$$

v_{TH} is unidirectional thermal velocity and is defined $v_{TH} = \sqrt{(2k_BT/\pi m^*)}$. At zero temperature, $v_B = 2qL_c/(\pi m^* v_f)$ where v_B and v_f are ballistic mobility under nondegenerate conditions and Fermi velocity of electrons [17].

From the scattering theory of MOSFET under ballistic limit, the drain current (I_{DS}) is defined as[17,18]

$$I_{DS} = \frac{\lambda}{\lambda + L_c}I_{ballistic} \quad (13)$$

Where λ is the mean- free path for carriers and L_c is the channel length. Under nondegenerate condition, Einstein relation gives the electron mobility $\mu_o = (q/k_BT)D_n$, where $D_n = (v_{TH}\lambda)/2$ the diffusion coefficient. Using these expressions, we find

$$\mu_o = \frac{q\lambda v_{TH}}{2k_BT} = \frac{q\lambda}{\pi m^* v_{TH}} \quad (14)$$

Under nondegenerate condition $\mu_B = qL_c/(\pi m^* v_{TH})$ and we have following relation

$$\frac{\lambda}{\lambda + L_c} = \frac{\mu_o}{\mu_o + \mu_B} \quad (15)$$

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Under degenerate condition drain current equation is modified as

$$I_{DS} = \frac{\alpha\lambda}{\alpha\lambda + L_c} I_{ballistic} \qquad (16)$$

At the diffusive limit ($L_c >> \lambda$), we have $I_{Ds} = (\alpha\lambda/L_c) I_{ballisitic}$. Under non degenerate condition α=1 and Equation -16, became same as Equation -13.At zero Kelvin temperature, α=2/3. This result is consistent with the quasi-ballistic transport theory at zero temperature (Note that L_o should be equal to 2λ/3 according to definition) [18].

V. Effect Of Strain On Ballistic Transport

With strain, the injection velocity shows a slight increase even if the effective transport mass remain unchanged. This is due to strain-induced splitting the conduction band into lower and heaver mass of electron, resulting the ratio of light electron in carriers increases and so the average injection velocity[19].

VI. Self-Heating Effect (SHE) in Strained Silicon MOSFET

Heat generation in ultra- short/Nanoscale devices is found to occur almost entirely in the drain, beyond the peak electric field regime when transport across the channel is quasi- ballistic. The heat generation region(“hot spot”) extends deep into the drain, because the energetic electrons spend relatively long time and devote their energy to the lattice and consequently it got partially in the drain region [21].

One of major issues concerning strained- silicon MOSFETs is the self- heating problem. Since thermal conductivities of the $Si_{1-x}Ge_x$ alloys (~5-10W/m-K) and SiO_2 dielectric (~1 W/m-K) layer are much smaller than that of bulk silicon, therefore strained silicon devices are potentially more prone to self- heating comparing to conventional MOSFETs. In addition, it is well established that conductivities of silicon layers of thickness less than 300 nm are significantly less than the bulk values, due to photon – boundary scattering . The effect of phonon – boundary scattering has been investigated through the measured reductions in lateral thermal conductivity compared to the bulk value. The measured lateral thermal conductivity of a 20 nm thin silicon film at room temperature can be as small as 24 W/m-k[15].

This can further impend the heat conduction from the device and subsequently exacerbate_the self – heating [8,20]

Table-1 shows, Thermal conductivities of a few materials used in device fabrication. Heat conduction in all materials is by phonons. The energetic electron releases their extra energy in terms of phonons. At Si/ $Si_{1-x}Ge_x$ interface, due to difference in thermal conductivities phonon scattering occurs which significantly increase the temperature. [21]

Table.No.1

Material	Thermal Conductivity(W/m-K)
Si(Bulk)	148
Ge(Bulk)	60
Slicides	40
$Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_2$	8/5
SiO_2	1.4

From above table-1it is clearly shows strained – Si transistor facing more self- heating problem because thermal conductivities of the $Si_{1-x}Ge_x$ alloys (~5-10W/m-K) and the SiO_2 dielectric (~1W/m-K) layer are much smaller than the conductivity of bulk silcon (148W/m-K), [22]

VII. Conclusion

The quasi-ballistic/ ballistic transport characteristic is re-examined for Nanoscale MOSFET as well for strained silicon MOSFETs. We observed that for smaller channel length backscattering coefficient is smaller means that ballistic efficiency is larger and drain current is also larger for same applied external condition. We also observed that strained silicon MOSFET is more pron to self heating due to lower thermal conductivity as compared bulk MOSFET. This self – heating problem reduces the drain current and also transconductance in Nanoscale dimensions.

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BIOGRAPHY

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