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ORIGINAL PAPER

Low Power Circuit and System Design Hierarchy and Thermal Reliability of Tunnel Field Effect Transistor

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Abstract
Tunnel FET is one of the promising devices advocated as a replacement of conventional MOSFET to be used for low power applications. Temperature is an important factor affecting the performance of circuits or system, so temperature associated reliability issues of double gate Tunnel FET and its impact on essential circuit design components have been addressed here. The temperature reliability investigation is based on double gate Tunnel FET, containing $Si_{1-x}Ge_x$ /Si, source/channel and HfO_2 high-k gate dielectric material. During investigation, it has been found that at high temperature application range ~ 300 K - to - 600 K,the Tunnel FET device design parameters exhibit weak temperature dependency with switching current (I_{ON}), while the off-state current (I_{OFF}) is slightly varying ~10^{-17}A/μm-to-10^{-10}A/μm. In addition, the impact of temperature on various device design element such as V_{TH}(i.e.,switching voltage),on-current (I_{ON}), off-current (I_{OFF}), switching ratio (I_{ON}/I_{OFF}) and average subthreshold slope (i.e., SS_{avg}), ambipolar current (I_{AMB}) have been done in this research work.The essential circuit design components for digital and analog/RF applications, such as current amplification factor($g_{m)}$ and its derivative (g_m'),the C-V components of device design, Cgg, Cgd and C_{gs}, cut - off frequency (f_T) and gain band width (GBW) product have deeply investigated. In conclusion, the obtained results show that the designed double gate Tunnel FET device configuration and its circuit design components are suitable for ultra-low power circuit,system applications and reliable for hazardous temperature environment.

Keywords Tunnel FET · Thermal reliability · $Si_{1-x}Ge_x$ · System MOSFET · Analog/RF

1 Introduction

In the last few years, anaggressive research toward Tunnel FET based circuit and system has been recorded due to existing threats to the conventional MOSFET for ultra-low power applications. The reason behind attraction of semi conductor player and low power design engineers areits low leakage-current, steeper sub-thresholdslope,SS < 60 mV/decade at room temperature (RT = 300 K) and lesser SCEs [1–4].The popular steep sub - threshold slope Field Effect devices such as Tunnel FET and Negative Capacitance Field Effect Transistor (NC FET) are most common between low power design engineers. However, due to reliable conventional CMOS process technology, Tunnel FET has gain better place than other steep slope FET devices [1–12]. Another reason of attraction is it allows further scaling of power supply (V_{DD}), over rule on conventional FETs [9–18]. Moreover, for the perspective of applications purpose in hazardous thermal environment, Tunnel FETs behavioral investigation, in some extreme conditions (where the operating temperature such as furnace temperature, satellite communication military, medical sector aerospace etc.), it is important [15–23].

The abilities of Tunnel FET make a suitable candidate for replacement of conventional MOSFETs in various advanced power saving applications such as IoTs (i.e. Internet of things) and portable electronics. Inthe Tunnel FET,the transport phenomenon occurs due band- to- band tunneling(B2B),governed by Kane'sModel [1–10].This device shows smaller value off-state current(I_{OFF})than conventional MOSFET at similar

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operating conditions. Due to the B2B tunneling transport mechanism and larger band width ($E_G \approx 1.12$ eV), silicon-based Tunnel FET, shows smaller on-state current (I_{ON}) than conventional MOSFETs [10–25].Taking care of these limitations of conventional silicon- based MOSFET and Tunnel FET structures, we have adopted double gate Tunnel FET (DG Tunnel FET) containing high-k gate dielectric materials, hafnium oxide(HfO_2, $k \approx 25$) and channel region has $Si_{1-x}Ge_x$ and Si. The interface of $Si_{1-x}Ge_x$ and Si in channel reduces the tunneling window pumps more charge carrier from valance band to conduction band in the device at same operating voltage, helps to improve the I_{ON}/I_{OFF} ratios. The tunable behavior of $Si_{1-x}Ge_x$ provides large design window for engineer and due to compactable process technology with conventional existing CMOS process technology helps to reduce production cost. As we know that almost all semiconductor devices show temperature dependency behavior, causes unstable performance with temperature variation [15–29]. Due to this, in this research work, we have considered as serious issues of temperature variation and its impact of circuit design matrix elements that is commonly used in high frequency(HF), low power applications. Remaining research report is classified the following sub-sections as:

2 Experimental Setup

All results of the double gate Tunnel FET, presented in this research report and circuit design elements have been carried outusing Silvaco/ATLAS device simulator version 3.1.20.1.R and MATLAB computational tool. The fine meshing tunneling in the regions where B2B tunneling mainly takes place were defined. The mesh size of 5×10^{-4} μm at interface source/channel and mesh size of 10^{-3} μm far of interface. The Tunnel FET structure used hereis shown in Fig. 1 and all its device design component and its values are collectively shown in Table 1. In the work, interface effect has not considered during analysis.

3 Results and Discussion

3.1 Device Design Topology

Fig. 1 shows the schematic diagram of double gate Tunnel FET (DG Tunnel FET). Table 1 summarizes all device design parameters that have been used during device simulation. For asymmetric source/channel staggered hetero tunnel junction, DG Tunnel FET, shown in Fig. 1, gate dielectric thickness (t_{ox}) is 2.0 nm and HfO_2 (k = 25) have been used. The thickness of silicon source channel has been taken 10.0 nm, while whole, channel length has been taken as 50.0 nm. A uniform doping of 1.0×10^{20} cm^{-3} and 5.0×10^{18} cm^{-3} have been used for the drain and source regions, respectively. The work function for gate material corresponding to this region has chosen 4.9 eV.The calibration of TCAD models with published work [Ref. 29] shows in Fig. 1(b).

3.2 Impact of Germanium (Ge: Mole Fraction(x))

Fig. 2 shows the impact of germanium contents ontransfer characteristic of double gate Tunnel FET shown in Fig. 1.The bandgap of $Si_{1-x}Ge_x$ semiconductor depends on the germanium contents, popularly known as mole fraction denoted as x.The germanium content in $Si_{1-x}Ge_x$and silicon causes a hetero interface state between two semiconductor materials, near the tunneling region in the device as shown in Fig. 2(a). The used term $E_{g\text{-effective}}$ band gap of $Si_{1-x}Ge_x$\ Si. In Tunnel FET device terminology known as effective tunneling window, travelled by charge carrier during transport in the device depends on germanium contents, x.The term ΔE_c is conduction band offset due misalignment of bandgap of $Si_{1-x}Ge_x$ and Si. The tunneling probability and effective resultant current is governed Wentzel–Kramers–Brillouin (WKB) quantum theory written by Eq. 1 [8]:

Table 1 device design component of double gate Tunnel FET

S.N.	Physical Parameters	Nomenclature (Unit)	Numericable value
1	φ_M	Work function (eV)	4.9
2	N_S	Doping levels for source (cm^{-3})	1.1×10^{20}
3	N_D	Doping level for Drain (cm^{-3})	5.1×10^{18}
4	N_C	Doping level for channel (cm^{-3})	10^{15}
5	t_{ox}	Gate oxide material thickness (nm)	2.0
6	L_t	Total length of the device (nm)	250.0
7	L_{ch}	Channel length (nm)	50.0
8	t_{Si}	Silicon film thickness(nm)	10.0
9	L_S/L_D	Source and drain lengths (nm)	100.0

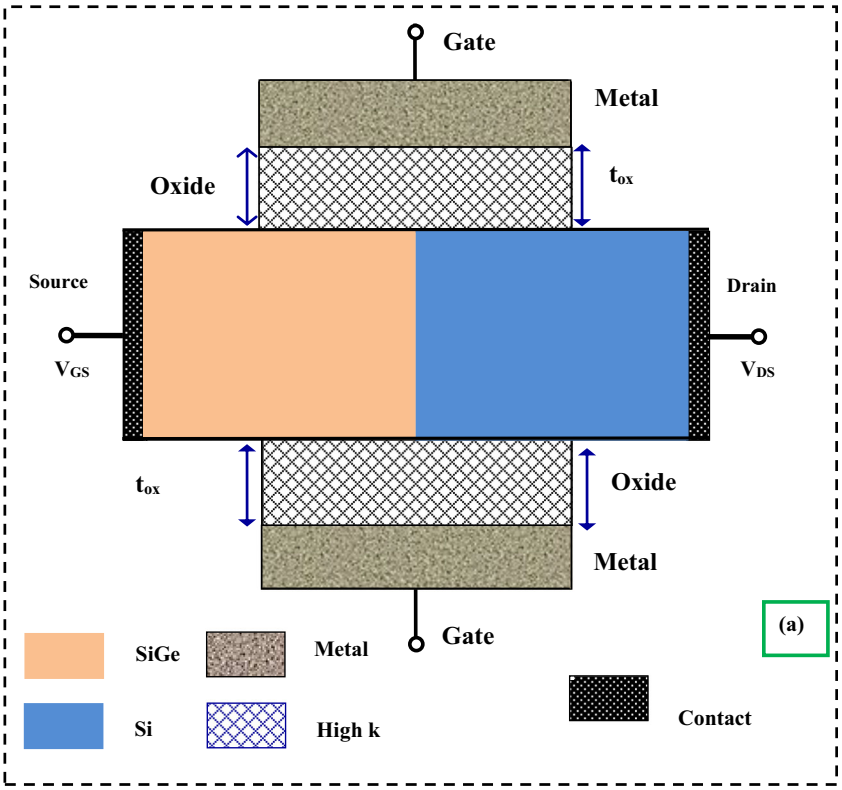
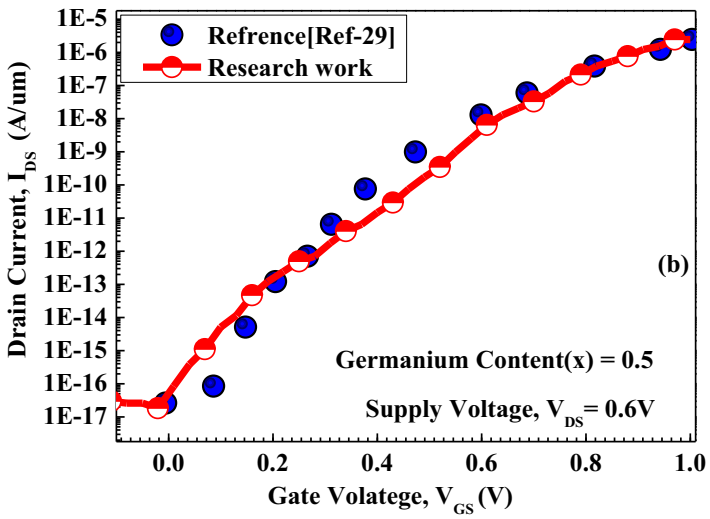


Fig. 1 schematic diagram of double gate Tunnel FET [Fig. 1(a)]. Fig. 1(b) Calibration of TCAD models with experimental published work



$$I_{DS}\sim T(E)\propto\left(-\frac{4\sqrt{2\,m^{*}}E_{g-effective}^{\frac{3}{2}}}{3|q|\overline{h}\left(E_{g-effective}+\Delta\varnothing\right)}\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}t_{si}}\right)\Delta\varnothing \quad (1)$$

In Eq. 1, the term m* is the effective mass of charge particle, $E_{g\text{-effective}}$ is effective band gap, $\Delta\Phi$ is the energy range for band to band tunneling (B2BT) window through which, the carrier's tunnel from one side to the other. The TFET device design matrix variables t_{ox}, t_{si}, $\varepsilon_{ox}$and ε_{si} are, the oxide and silicon films thickness and dielectric constants respectively. The remaining constant such as "ħ" is called as the reduced Planck's constant and "|q|" is the electronic charge. The tunneling window ($\Delta\varnothing$) in the tunneling probability can be also expressed as: $\Delta\varnothing = E_V^{ch}-E_C^S$. The involvement of Ge causes tunable tunneling window for device and completely controlled by process engineer. These provide wider facilities range of device design for applications.It is evident from Fig. 2 (b) that, the switching current, I_{ON} depends on Ge content. This is due to tunable behavior and depends on germanium contents, x. The extracted device

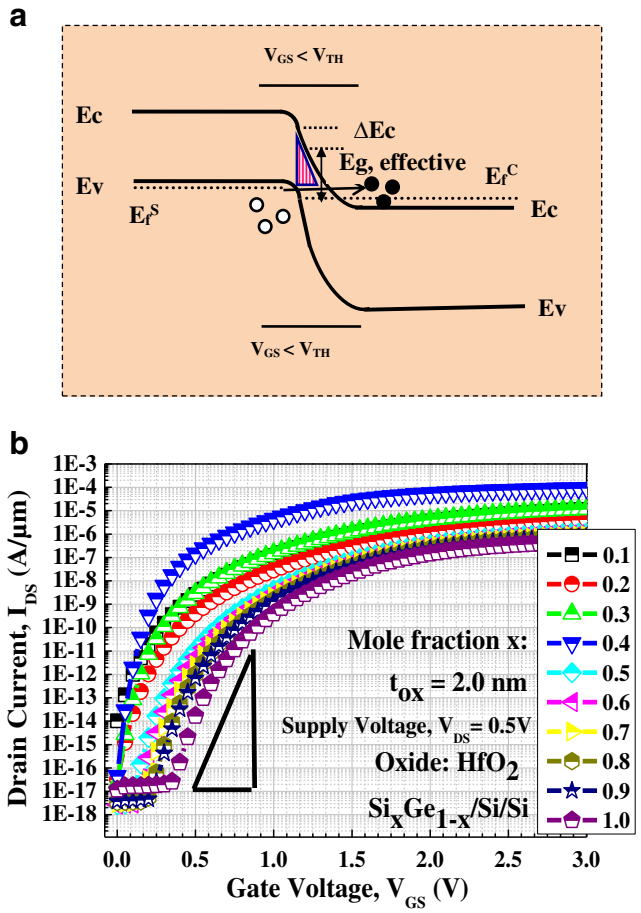


Fig. 2 (a) Energy bandgap and band offset representation of schematic diagram inside the Tunnel FET. The term Ec: Conduction band, Ev: Valance band, V_{TH}: Threshold Voltage, E_f: Fermi Level under non equilibrium, **(b):**transfer characteristic for double gate Tunnel FET and représentation of impact of germanium contents at room temperature (RT = 300 K)

design parameters of DG Tunnel FET are resumed in Table 2. The best results are obtained around 40% Ge content. The larger amount of Ge contents causes negative impact in the since of slight increase in I_{OFF} and reduced I_{ON}. As shown in Table 2, for 40% Ge, Tunnel FETshows best performance in the sense of I_{ON},I_{OFF}, I_{ON}/I_{OFF} and average subthreshold slope (SS_{Avg}) calculated by Avg−SS = $V_{VD}/\log(^{I_{ON}}/_{I_{OFF}})$ [2].

As shown in Table 2, device design parameters such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF},SS_{Avg} are controlled by germanium contents, x. The investigation summary, shown in Table 2, reports that optimum value of device design parameters is obtained for 40% germanium contents. The one of useful information of Table 2 is for process and design engineer have large window for development of circuit and systems according to user demands. The average subthreshold slope of design device is decreasing with higher value of germanium contents, this is due to reduction of bandgap causes more current pumping form source to drain via channel, while off-state current variations are very less. These forces for optimization of I_{ON}/I_{OFF} ratio and SS_{Avg}, as shown in Table 2.

3.3 Impact of Temperature Variation

This section is center part of this research work. As defined in the problem definition that thermal management is always a challenging task for a circuit and system developer. In nanotechnology, thermal management is becoming more critical day by day. For more practical and compact system development, thermal analysis and management at each level such as device, circuit and system are essential. Proper choice of device and circuit always helpful for managing thermal issues. Looking the practical applications, this section reports a depth analysis of thermal effect on device level and its impact on circuit design elements.

The device design components of DG Tunnel FET such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF},threshold voltage (V_{TH}) and average subthreshold slope (SS_{Avg})is shown in Fig. 1 is resumed in Table 3. The best device design feature(I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, (V_{TH}) and SS_{Avg}) has been obtained for room temperature (RT = 300 K). From Table 3, it has been observed that as temperature increases, the threshold voltage (V_{TH}) and average sub threshold (SS_{Avg}) slightly increases due slight

Table 2 Extracted circuit design parameters of DG Tunnel FET

Mole fraction (x)	I_{OFF} (A/μm)	I_{ON} (A/μm)	I_{ON}/I_{OFF} ratio	SS_{Avg}(mV/decade)
0.1	1.02×10^{-17}	1.13×10^{-5}	1.10×10^{9}	55.28
0.2	3.25×10^{-17}	4.23×10^{-6}	1.30×10^{11}	44.98
0.3	2.33×10^{-17}	1.18×10^{-5}	5.05×10^{11}	42.72
0.4	4.53×10^{-17}	9.36×10^{-5}	2.06×10^{12}	40.60
0.5	2.69×10^{-18}	1.14×10^{-6}	4.23×10^{11}	43.00
0.6	2.64×10^{-18}	9.98×10^{-7}	3.77×10^{11}	43.19
0.7	3.10×10^{-18}	8.73×10^{-7}	2.81×10^{11}	43.66
0.8	3.53×10^{-18}	7.62×10^{-7}	2.16×10^{11}	44.11
0.9	3.76×10^{-18}	7.13×10^{-7}	1.89×10^{11}	44.33
1.0	1.19×10^{-18}	4.74×10^{-7}	3.97×10^{10}	47.17

Table 3 Impact of temperature variation on device design parameters

Temperature (K)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF} ratio	(V_{TH}) (V)	$SS_{Average}$ (mV/decade)
300	9.29×10^{-5}	4.32×10^{-17}	2.15×10^{12}	0.51	40.54
350	8.96×10^{-5}	1.04×10^{-16}	8.59×10^{11}	0.51	41.89
400	8.57×10^{-5}	1.78×10^{-15}	4.79×10^{10}	0.52	46.81
450	8.21×10^{-5}	2.63×10^{-14}	3.11×10^{9}	0.52	52.66
500	7.85×10^{-5}	4.89×10^{-13}	1.60×10^{8}	0.53	60.93
550	7.51×10^{-5}	8.43×10^{-12}	8.91×10^{6}	0.54	71.94
600	7.19×10^{-5}	1.05×10^{-10}	6.82×10^{6}	0.55	85.69

variation in I_{OFF},and weaker dependency of used semiconductor energy band diagram with temperature noticed from Fig. 3. The weaker dependency of $Si_{1-x}Ge_x$ and Si causes lightly variation in threshold voltage of DG Tunnel FET with temperature increment. It causes additional band alignment with applied adoptable due to inherent weak temperature dependency with energy bandgap.As shown in Fig. 1 (b) rectangular area color indicates the point subthreshold slope (SS_{Point}) is defined byEquation2:

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_G}\right)^{-1} \quad (2)$$

is function of germanium content, x in $Si_{1-x}Ge_x$.Fig. 1(b) indicates that as germanium content in $Si_{1-x}Ge_x$increases SS_{Point} is also deceasing. The reverse effect of germanium content and SS_{Point} indicates that, it also helps in the reduction of supply voltage with optimum performance.

Figure 3 shows, the typical transfer (I_{DS}-V_{GS}) characteristic of the device, shown in Fig. 1 and the impact of temperature variations. From Fig. 3, it has been observed that for temperature ~ 300 K –to- 600 K, the I_{ON} variation is ~9.29×10^{-5} A/μm to ~7.19×10^{-5}A/μm.The variation of I_{OFF} is ~10^{-17}A/μm-to-10^{-10}A/μm for temperature range ~ 300 K - to - 600 K. But for practical point of view, these variations are adoptable. The reduction of band gap due temperature also causes unwanted slight instability effects on the device performance.

The impact of temperature variation on threshold voltage, (V_{TH})of device is shown in Fig. 4. The (V_{TH}) slightly varies ~0.51 V- to - 0.55 V for temperature range ~ 300 K- to - 600 K, shown in Fig. 4. The slight variation (V_{TH}) is an indication of insensitive response of device in hazardous temperature environment and indication reliable response. Fig. 5 shows the impact of temperature on switching ratio I_{ON}/I_{OFF} and average subthreshold slope SS_{avg}. Fig. 6 shows the sensitivity analysis of device with temperature variation defined by $d(I_{ON})/dT$ and $d(I_{OFF})/dT$. Temperature sensitivity of I_{ON} and I_{OFF} is around 500 K is neglable. Small variation is obtained after 500 K.

Figure 7 shows that ambipolar behavior of device shown in Fig. 1. The ambipolar current is rapidly increasing for applied temperature range.

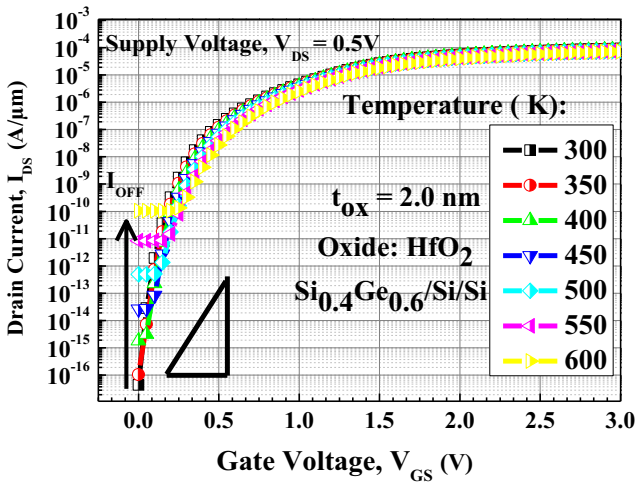


Fig. 3 I_d-V_g characteristics for double gate Tunnel FET and représentation of impact of température variation for 40% germanium content

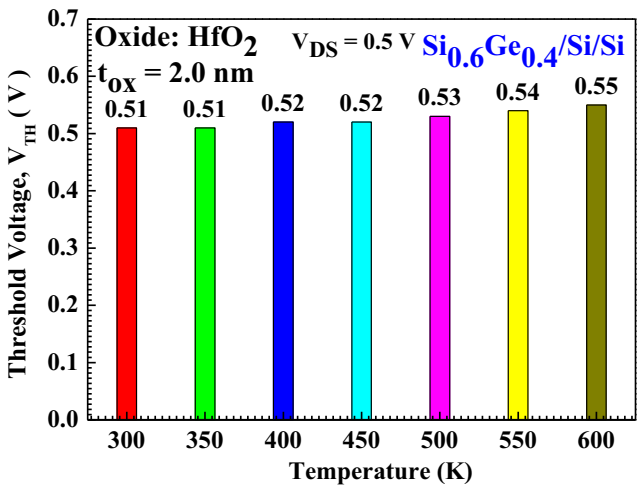


Fig. 4 Impact for temperature on threshold voltage of double gate Tunnel FET

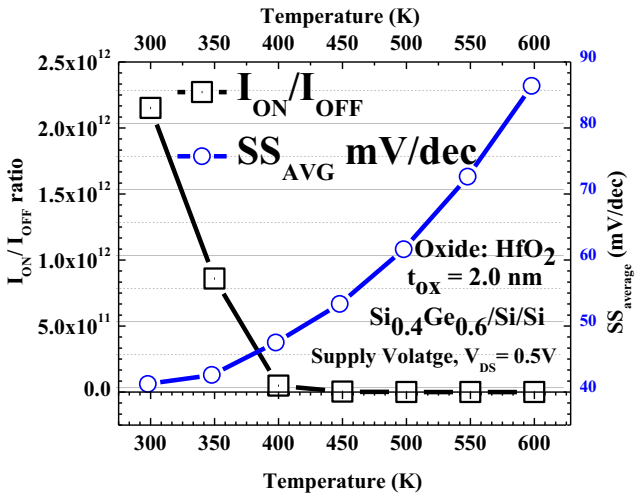


Fig. 5 impact of temperature on I_{ON}/I_{OFF} ratio and average sub threshold slope of double gate Tunnel FET

4 Circuit Design Topology

4.1 Digital Circuit Design Topology

Figure 8 shows the variation of $g_m$with applied gate voltage V_{GS} and impact temperature on it. It is evident from figure that,the DG Tunnel FET exhibits slightly reduction in the g_m values with temperature variation.This is due to weaker dependency of bandgap with temperature. The variation of $g_m \sim 6.11 \times 10^{-5}$S/μm -to- 4.59×10^{-5}S/μm for temperature range ~300 K- to - 600 K. Fig. 8 shows the g_m versus $I_{DS}$and temperature impact on it. This weaker dependency indicated insensitive behavior of device. As shown in Fig. 9, the left flanks of the curves overlap i.e. the amplification is the same whatever the temperature varies. An offset Δg_m has been observed on the right side of the curves. This offset results in the cutoff frequency. Its higher order derivative of g_m shown in Fig. 9. This means the amplification decreases but of a very weak influence on the device. The same observation has been observed in Fig. 7. From Fig. 9 and Fig. 10, it has

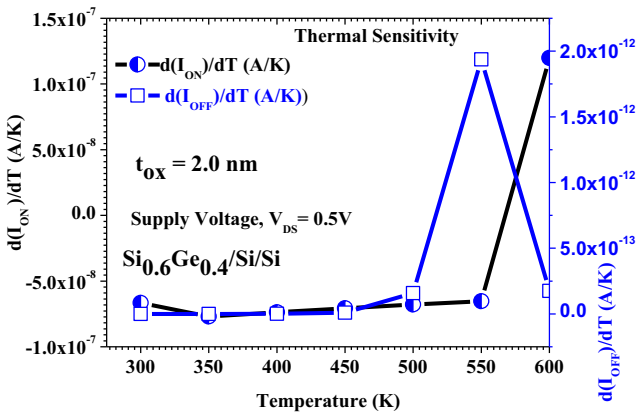


Fig. 6 impact of temperature sensitivity on I_{ON} and I_{OFF} of double gate Tunnel FET

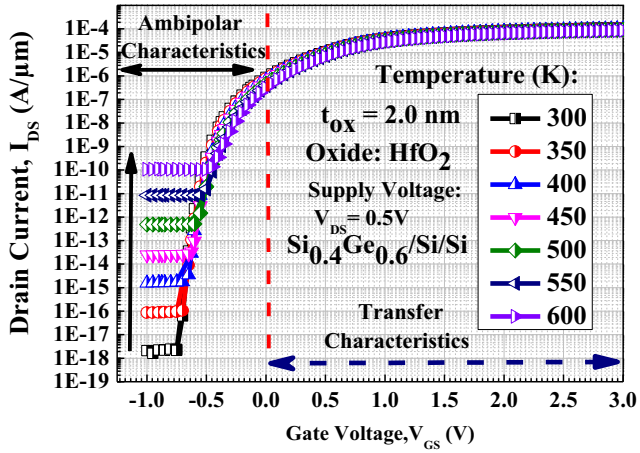


Fig. 7 transfer\ambipolar characteristics for double gate Tunnel FET and représentation of impact of température variation

been being noticed that, the variation in temperature does not affect the performance and reliability of the device. The shift of the maximum of g_m is small and results are resumed in Table 4.

4.2 Analog/RF Circuit Design Topology

The C -V characteristic of DG Tunnel FET is useful in the analysis of the frequency response (RF) and switching characteristics of the low integrated circuits. Figure 11 shows impact of temperature and input voltage V_{GS} on C-V components, of device design: C_{gg}, C_{gd} and C_{gs}. An increase in capacitance from bottom to top at the threshold voltage, the Gate-Gate capacitance (Cgg) is mainly composed of two capacitances, gate-drain (Cgd) and gate-source (Cgs). As, we know that, the gate-source capacitance (Cgs) is lower because of the presence of the tunnel effect, the gate-drain capacitance (Cgd) is a dominant capacitance due to the accumulation of the electrons of the channel-source and collected by the drain

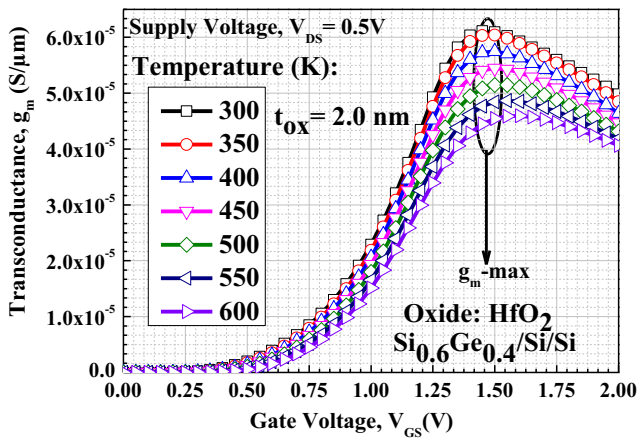


Fig. 8 g versus V_{GS} characteristic and impact temperature of double gate Tunnel FET

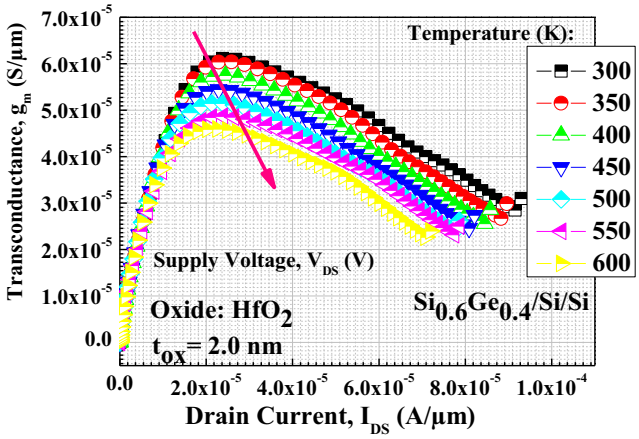


Fig. 9 g versus I_{DS} characteristic of double gate Tunnel FET and impact of temperatur

region. In this section, the thermal effect on C-V components of device is shown.

For investigation of C-V characteristics and its responses with temperature variation, the gate of the DG Tunnel FET is supplied by an alternative signal AC at frequency equal to 1 MHz and a DC voltage of a few mili voltages. The simulated results show that are a negligible influence of temperature on the total Cgg, Cgdand $C_{gs}$of the transistor, shown in Fig. 11.Moreover, the cut-off frequency (f_T) and gain bandwidth (GBW) product of n-channel DG Tunnel FET are much larger than that of conventional DG Tunnel FET, which is due to the excellent DC characteristics. It has been evaluated by the ratio of g_m to Cgg, with following relation, Eq. 3.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{g_m}{2\pi C_{gg}} \tag{3}$$

As shown in Fig. 12, as V_{GS} increases, the cut-off frequency (f_T) increases to reach its maximum on left Y-axis, then the

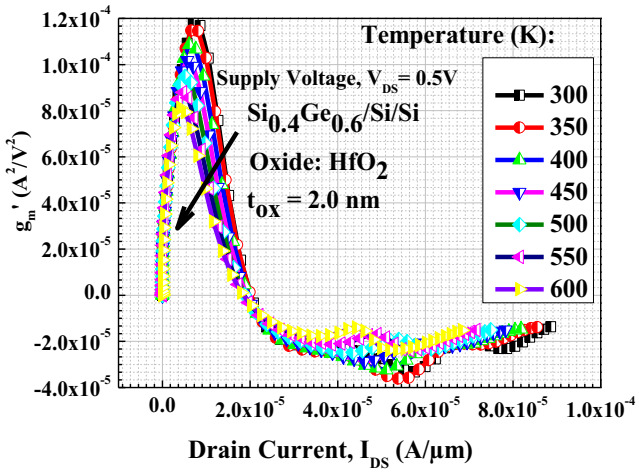


Fig. 10 derivative of g_m- I_{DS}characteristic double gate Tunnel FET and impact of temperature

Table 4 Extracted device parameters forAnalog/RF design matrix parameters

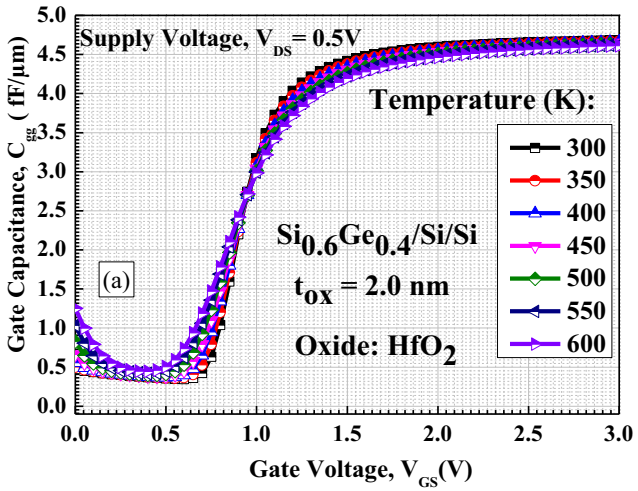
Temperature (K)	Maximum of g_m (S/μm)	Maximum of f_m (GHz)	Maximum of GBW(GHz)
300	6.11×10^{-5}	2.51	0.86
350	6.04×10^{-5}	2.12	0.62
400	5.75×10^{-5}	1.92	0.41
450	5.45×10^{-5}	2.02	0.27
500	5.15×10^{-5}	1.72	0.20
550	4.87×10^{-5}	1.82	0.19
600	4.59×10^{-5}	1.72	0.18

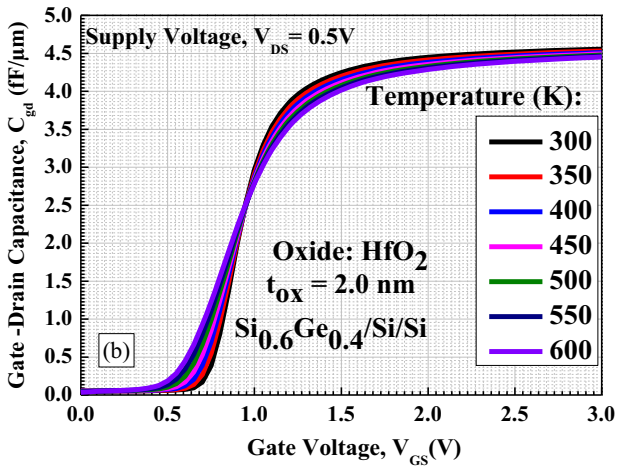
increasing Cgg, start goes down, as soon as the gate voltage reaches 1.0 V. The cut-off frequency (f_T) varies slightly with V_{GS} at1.0 V. This is because in on-state current and g_m value increases with the band to band tunneling.The cut-off frequency (f_T) of DG Tunnel FETshown Fig. 1 is the largest at temperature 300 K due to large tunneling current and g_m.

The gain bandwidth product (GBW) is another important analog/ RF circuit design parameter is calculated by the Eq. 2. Fig.12 shows the impact of applied input voltageV_{GS} on the GBW on right Y-axis.The GBW increases with the increase in the gate voltage (V_{GS}) until it reaches a maximum ~0.7 V after that it decreases as soon as the gate voltage V_{GS} is close to the threshold voltage (V_{TH}) of the n-channel DG Tunnel FET. The similar variation for the cut-off frequency (f_T) versus applied V_{GS} has been obtained. The curves of the cut-off frequency (f_T) the peak of the gain is better for a temperature 300 K.

The maximum values of the g_m, cut-off frequency (f_T), gain bandwidth product (GBW) and its impact on temperature are extracted for double gate Tunnel FET has summarized in Table 4. The extraction circuit design component and analysis of circuit design matrix parameters has done for 40% Ge contents. From Table 4, it has observed that there are slight variations in $g_{m\text{-}max}$, f_{T}-Max and GBW for temperature 300 K -to-600 K. This indicate that the increase in temperature does not affect on these desirable circuit design parameters, despite there is a slight impact on the offset of the peak's electrical parameters (Fig. 13).

The histogram of DG Tunnel FET shown in Fig. 14. shows the variation of cut-off frequency (f_T) versus applied gate voltage (V_{GS}) and impact of temperature variation for supply voltage, V_{DS} = 0.5 V. A slight degradation of the maximum, cut-off frequency has been observed, therefore the bandwidth decreases which confirms the simulated curve of Fig. 14. The histogram shown in Fig. 14 clearly shows the impact of temperature on the peak of the cut-off frequency (f_T). The best peak is reached for a temperature equal to 300 K. When the temperature is increased the amplification decreases the band of work in the alternative regime decreases.





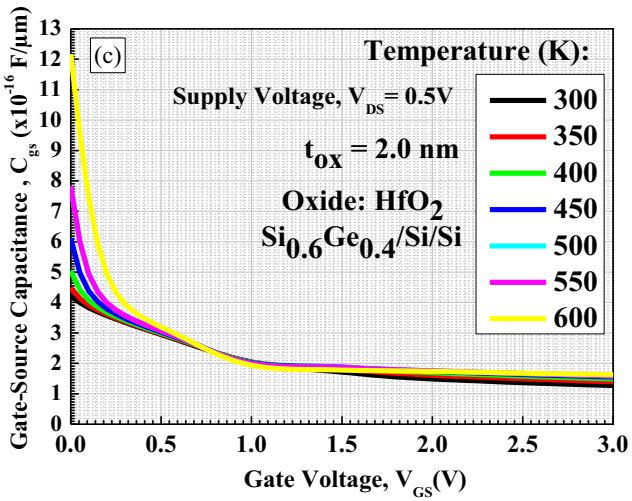


Fig. 11 Impact of temperature and input voltage V_{GS} on C-V components, of device design Cgg (a)C_{GD} (b) and C_{GS}(c)

$$GBW = \frac{g_m}{2\pi\ 10\ C_{gd}} \tag{4}$$

Fig. 15. shows the variation of gain band width (GBW) product versus applied gate voltage (V_{GS}) and impact of

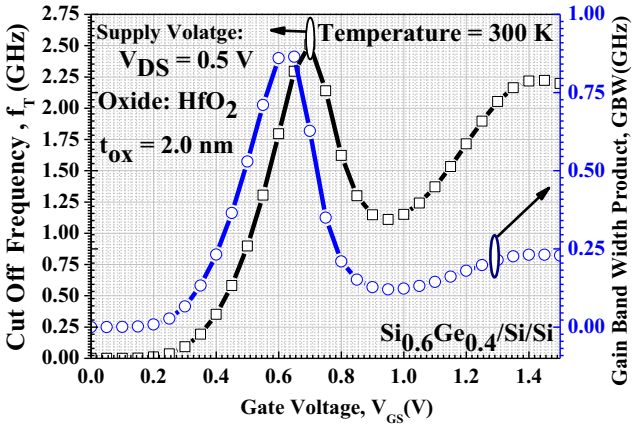


Fig. 12 variation of cut-off frequency and gain band width versus applied V_{GS}

temperature variation for supply voltage, V_{DS} = 0.5 V. The GBW is slightly decreasing with temperature, indicates weak dependency. At device thermal sensitivity on circuit component is adoptive. However, in SLSI (super-large-scale integration) applications, these sensitivities cannot ignore. These increases responsibilities of circuit and system design engineers.

As known in Eq. 2 and 3, f_T, GBW depends on multivariable such g_m and Cgg.For understanding the composite effect on it, Fig. 16 and Fig. 17 presented here. Fig. 16 and Fig. 17, shows impact of applied gate voltage (V_{GS}) on transconductance (g_m) cut off frequency (f_T) and gain band width (GBW) product in 3-D. These Fig. 16 and Fig. 17, extracted from Atlas and plotted in MATLAB show the relation between V_{GS}, transconductance (g_m), gain band width (GBW) product and cut off frequency (f_T) for $Si_{1-x}Ge_x$ based digital, analog/RF performance parameters. The result report has been recorded for 40% germaniums content with supply voltage V_{DS} = 0.5 V for room temperature (RT) = 300 K. The 3-D plots for cut off frequency (f_T) and GBW is plotted in investigation multivariable input voltage V_{GS} and g_m followed by Eq. 1 and 2. These results show the inter dependent relation

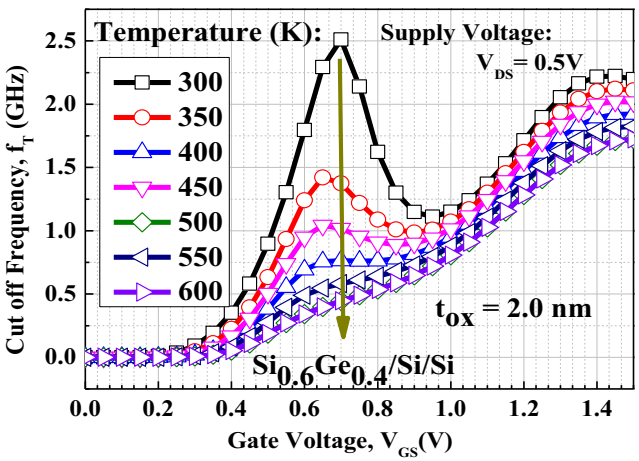


Fig. 13 variation of cut-off frequency(f_T) versus applied gate voltage (V_{GS}) and impact temperature variation

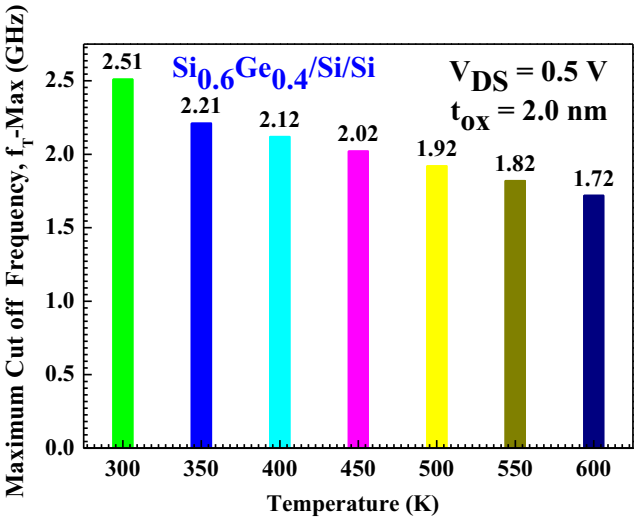


Fig. 14 impact temperature variation in maximum cut-off frequency (*f*max)

between the circuit parameters; provide better performance optimization opportunities for design engineers. It has been concluded that these figures in 3D shown in Fig. 16 and Fig. 17, confirm a linear relationship between the 3 parameters (V_{GS}, g_m, and GBW) followed by Eq. 3 and 4.

5 Conclusion

In this research work, it has been investigated the temperature reliability of DG Tunnel FET and its impact on device and circuit design elements for low power applications.It has been observed that, the impact of temperature on various device design element such as V_{th} (i.e., switching voltage) I_{ON}(i.e., switching current), I_{OFF}(i.e., leakage current), switching ratios (I_{ON}/I_{OFF}) and average subthreshold slope(i.e., SS_{avg}).In conclusion, it has been observed that, at large temperature

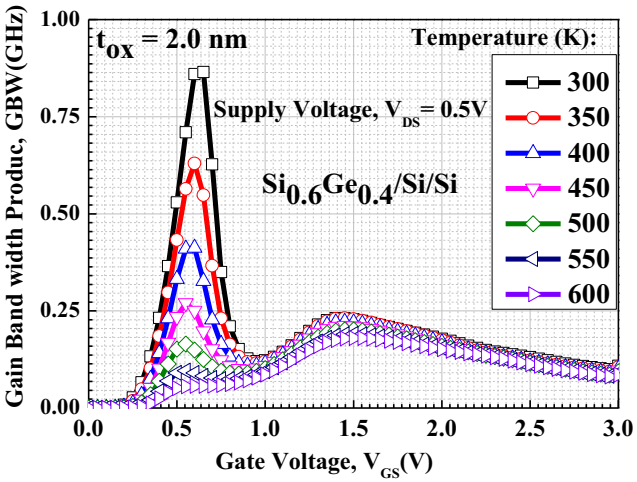


Fig. 15 impact of temperature variation in gain band width (GBW) product versus V_{GS}

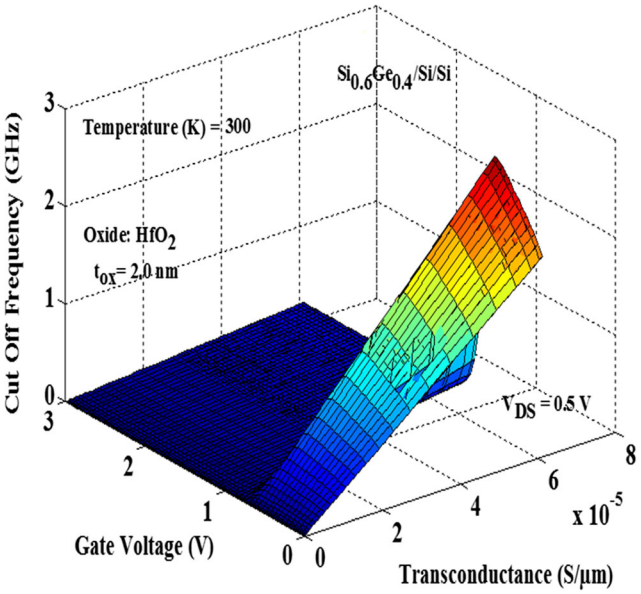


Fig. 16 impact of V_{GS} on g_m and cut off frequency (f_T) in 3 D variation

application range ~ 300 K - to - 600 K, the design parameters exhibit weak temperature dependence with switching I_{ON}, while I_{OFF} is slightly increase ~10^{-17}A/μm-to-10^{-10}A/μm. The impact of temperature in V_{th} is adoptable due to large thermal variations.The ambipolar current found in designed device structure is little bit more sensitive with thermal variations.In the advancement of this research for circuit and system design, we have thoroughly investigated the impact of temperature variations on its circuit design matrix components for digital and analog/RF applications. The obtained results such as g_m, its derivative (i.e.,g_m, f_T, f_{max}, GBW product have superior responses due insensitive response with low temperature variation.The response of this research is excellent. For

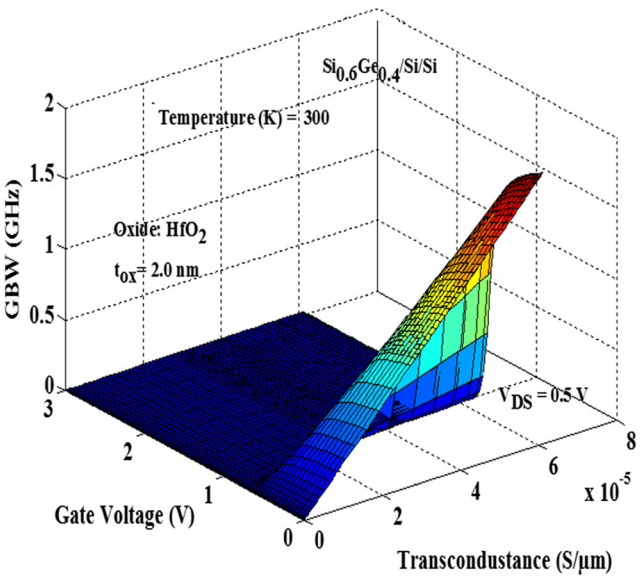


Fig. 17 impact of V_{GS} on g_m and gain band width(GBW)product in 3 D variation

low temperature applications like home appliances, IoTs, wearable applications, Tunnel FET is most suitable for power saving regime. For large thermal applications, Tunnel FET response is also adoptable.

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Author Contributions All included authors in the research manuscript have equal contribution.

Availability of Data and Material Data and materials are original work of authors.

Declarations

The procedure followed in this work is in accordance with ethical standards. This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to Participate None.

Consent for Publication None.

Conflict of Interest There is no conflict of interest from others.

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