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ORIGINAL PAPER

Analytical Compact Model of Nanowire Junctionless Gate-All-Around MOSFET Implemented in Verilog-A for Circuit Simulation

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Abstract
In the present research article, we have proposed an analytical compact model for nanowire Junctionless Gate-All-Around (JLNGAA) MOSFET validated in all transistor's operation regimes. The developed model having an analytical compact form of the current expressions, based on surface potential (Φ_S), obtained from approximated solutions of Poisson's equation. The proposed model has implemented in standard Verilog-A language using SMASH circuit simulator in order to be used in various commercial circuit simulators. The proposed model has also validated using ATLAS-TCAD simulation for various physical parameters such as the channel doping concentration (N_d) and the channel radius (R) of JLNGAA MOSFET. Finally, based on the developed Verilog-A JLNGAA MOSFET model, we have tested it in four types of low voltage circuits, CMOS inverter, CMOS NOR-Gate, an amplifier and a Colpitts oscillator.

Keywords Nanowire · Junctionless · Gate-all-around MOSFET · Analytical compact model · Verilog-a · Digital circuit · Analog circuit

1 Introduction

In recent years, the CMOS technology has reached its physical limits [1–3] and as a consequence, the junctionless nanowire gate-all-around (JLNGAA) MOSFET has been drawing substantial research attentions [4–12]. With respect to the classical inversion mode transistors [13, 14], the JLGAA MOSFET offers excellent ability on gate control to reduce short-channel effects (SCEs), near ideal subthreshold slope (SS), higher ratio of Ion/Ioff, low-frequency noise (LFN) behavior, and lower gate tunneling probability [15–18]. Moreover, since the junctionless (JL) transistors eliminate the concept of ultrathin junctions, making these types of devices easier to fabricate and to down-scale [19–21]. For these reasons, the JLGAA MOSFET is considered as the best JL multiple-gate transistors for the future CMOS circuit implementation [22–24].

On the other hand, analytical compact models of JLGAA MOSFET adapted for various circuit simulators, are required for future use of these types of transistors in different kinds of integrated circuits. Besides, these types of model must be characterized by a simple, accurate and explicit analytical formulation [25].

In this context, several works have been completed for establishment of analytical compact model of JLGAA MOSFET [26–32], however a few of them have been implemented in Verilog-A language for future application in commercial circuit simulators to designs analogs and digitals circuits. Only one model has been implemented in Verilog-A language [33], and it is not dedicated to nanowire transistors. Also, it is a charge-based model (CBM) and not a surface-potential-based model (SPBM). The second approach (SPBM) provides excellent accuracy and more physical

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description of the device behavior and it is normally accepted in various analytical compact modeling applications. However, the derivation of SPBM is directly related to Poisson's equation solution, which is a complex mathematical operation in the case of JLGAA MOSFET, and it involves, in the general case, the using of Bessel function for the determination of the electrostatic surface potential in the channel Silicon.

In this work, we propose an analytical compact model for nanowire JLGAA MOSFET and its implementation in Verilog-A which can be useful for circuit simulation application. The developed drain-current expression models the electrostatic surface potential for each transistor's operation mode. It is derived from Poisson's equation using a regional approach and separated considerations, especially without using of Bessel function. We incorporate the Verilog-A code in the SMASH circuit simulator and test it in a Colpitts oscillator and inverter. In addition, the proposed model has a physics-based concept and given in compact analytical closed form, also it is easy to use because there is no fittings parameters or analytical complex formulation.

In this work, it has been proposed an analytical compact model for nanowire JLNGAA MOSFET and its implementation in Verilog-A which will be useful for advanced circuit simulation, design and development.

The expression for I_{ds} current has been developed with the help of surface potential Φ_S, measuring method. This method solves Poisson's equation using a regional approach and separated considerations, especially without using of Bessel function. During compact model development, we have incorporated the Verilog-A code in the SMASH circuit simulator and test it in analog and CMOS circuits: CMOS inverter, CMOS NOR-Gate, Colpitts oscillator and amplifier circuit. The additional advantages of developed compact model are no fittings parameters and a simple analytical formulation because the model has been using physics-based concept. This indicates better accuracy with lesser complexity.

2 Electrostatic Potential and Drain-Current

Figure 1 shows the schematic representation of considered JLNGAA MOSFET including the device geometrical parameters, respectively, R is the silicon body radius, t_{ox} is the oxide thickness, and L is the channel length.

The model begins with the surface potential expression Φ_S derived from the analytical solution of the Poisson equation in fully depletion region that was obtained by Bart Sorée et al. [32]:

$$\Phi_S = V - \frac{qN_d}{4\varepsilon_{si}}\left(2(R-r_d)^2\ln\left(\frac{R}{R-r_d}\right) - r_d(r_d-2R)\right) \quad (1)$$

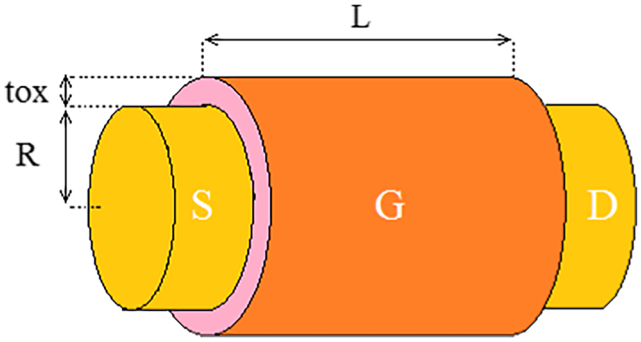

Fig. 1 Schematic view of 3D Junctionless N-types GAA MOSFET

where N_d is the channel doping concentration, ϵ_{si} is the permittivity of Silicon, q is the universal electronic charge of electron, and r_d is the depletion width and V is the potential shift due to the electron quasi-Fermi level. We can calculate the surface potential in Eq. (1) using the following gate boundary condition [34]:

$$C_{ox}\left(V_{geff} - \Phi_S\right) = -\varepsilon_{si}E_S \quad (2)$$

where $V_{geff} = V_{gs}\text{-}V_{fb}$ is the effective gate voltage, V_{gs} is the gate bias, $V_{fb} = \Phi_{ms} + \Phi_t\ln(N_d/n_i)$ is the flat-band voltage, E_s is the surface electric field, $C_{ox} = \epsilon_{ox}/R\ln(1 + t_{ox}/R)$ is the oxide capacitance, ϵ_{ox} is the permittivity of the oxide, Φ_{ms} is the workfunction (WF) difference between the metal-gate and channel semiconductor, n_i the intrinsic concentration, $\Phi_t(=KT/q)$ is the thermal voltage, K is the Boltzmann constant, T is the temperature.

We can't calculate the surface potential from Eq. (1) because it contains two unknown parameter, Φ_S (electrostatic surface potential) and r_d (depletion width). For that raison, we have eliminated parameter r_d from Eq. (1) in three main steps. First, at the interface between channel Silicon and Oxide, the surface electric field E_s is equal to $d\Phi/dr$ (for r = R) = $-Q_{tot}/\varepsilon_{si}$. Where $Q_{tot} = Q_m - Q_{dep}$ is the total charge density in the channel, Q_m is the mobile charge density and Q_{dep} is the fixed charge density [13, 34]. Second, when the device is biased in depletion region we can write $Q_{tot} \approx Q_{dep} \approx \prod qN_d(R^2\text{-}r^2_d)$ [31]. Combining $E_s = d\Phi/dr$ (for r = R) = $-Q_{tot}/\varepsilon_{si}$, $Q_{tot} \approx Q_{dep} \approx \prod qN_d(R^2\text{-}r^2_d)$ and Eq.2, we get $\prod qN_d(R^2\text{-}r^2_d) = Cox(V_{geff}\text{-}\Phi_S)$. Finally, injecting r_d (obtained from $\prod qN_d(R^2\text{-}r^2_d) = C_{ox}(V_{geff}\text{-}\Phi_S)$) in Eq. (1), we get an important relation for the surface potential Φ_S in deep depletion regime:

$$\Phi_S - V = \beta\left(V_{geff} - \Phi_S\right) + \left(2\beta\left(V_{geff} - \Phi_S\right) + \delta\right) \times \left(\ln(R) - \frac{1}{2}\ln\left(R^2\left(1 + \frac{2}{\delta}\beta\left(V_{geff} - \Phi_S\right)\right)\right)\right) \quad (3)$$

with $Q_{dep} = \pi qN_dR^2$ is the fixed charge, $\delta = Q_{dep}/2\pi q\epsilon_s$ and $\beta = C_{ox}/(4\prod\varepsilon_{si})$.

When the junctionsless transistor is biased in accumulation mode, the surface electric field can be approximated by Es≈ $\sqrt{2qNd\Phi t/\epsilon si[\exp((\Phi S-V)\ /\Phi t\ )-((\Phi S-V)\ /\Phi t\ )-1]}$ expression [35]. By applying the expression of E_s in Eq. (2), we get an important relation for the surface potential Φ_S and the voltages in the accumulation mode, as:

$$\Phi_S\left(\Phi_S-2V_{geff}\right)+V_{geff}^2=\eta\left(\exp\left(\frac{\Phi_S-V}{\Phi_t}\right)-1\right) \tag{4}$$

with $\eta = 2qNd\ \epsilon si\Phi t/Cox^2$.

In partly depleted regime, Eq. (3) can be written as:

$$\xi=\beta\left(V_{geff}-\Phi_S\right)+\left(2\beta\left(V_{geff}-\Phi_S\right)+\delta\right)\times\left(\ln(R)-\frac{1}{2}\ln\left(R^2\left(1+\frac{2}{\delta}\beta\left(V_{geff}-\Phi_S\right)\right)\right)\right) \tag{5}$$

with $\xi=-\Phi t[\exp((\Phi S - V)/\Phi t\ ) - ((\Phi S - V)/\Phi t\ ) - 1]$ inspired by the approximated solution of the surface electric field E_s in accumulation regime and it provides good agreement with the numerical simulation results. Moreover, Eq. (5) is related to the solution of E_s in deep depletion ($E_s = d\Phi/dr = -Q_{tot}/\varepsilon_{si}$, with $Q_{tot} \approx Q_{dep} \approx \prod qN_d(R^2\text{-}r^2_d)$) and also based on the approximated expression of E_s in the accumulation region [35].

For junctionless GAA MOSFET, the general expression of the drain-current I_{ds} can be written as [36]:

$$I_{ds}=2\pi\Phi_t\mu\frac{R}{L}\int_{V_s}^{V_d}\left[C_{ox}\left(V_{geff}-\Phi_S\right)+Q_{dep}\right]dV \tag{6}$$

By calculating the integral in Eq. (6) using $dV/d\Phi_S$ obtained from Eq. (3), then we get the expression of the current I_{ds} in deep depletion mode:

$$I_{ds}^{sub}=2\pi\Phi_t\mu\frac{R}{L}\times\left\{C_{ox}\left[i_c^p-\left(\frac{1}{2}+\left(\frac{1}{4}+\ln(R)\right)\beta\right)V_{geff}^2+\frac{1}{4}\delta V_{geff}+\left(\frac{3}{4}+\ln(R)+\frac{1}{2\beta}\right)\frac{\delta^2}{4\beta}\right]+Q_{dep}V\right\}_S^D \tag{7}$$

with,

$$i_c^p=\left(\left(\frac{\Phi_S}{2}-V_{geff}\right)\Phi_S+\frac{V_{geff}^2}{2}-\frac{\delta^2}{8\beta^2}\right)\beta\ln\left(\frac{R^2}{\delta}\left(\left(V_{geff}-\Phi_S\right)2\beta+\delta\right)\right)-\left(\left(\frac{1}{4}+\ln(R)\right)\beta+\frac{1}{2}\right)\Phi_S^2+\left(\left(1+\left(\frac{1}{2}+2\ln(R)\right)\beta\right)V_{geff}-\frac{\delta}{4}\right)\Phi_S$$

And, the current I_{ds} is calculated through the surface potential Φ_S evaluated at the source limits $\Phi_S(0)$ (with $V=V_s = 0.0$ V) and the drain limits $\Phi_S(L)$ (with $V=V_d$).

After calculating the integral in Eq. (6) using $dV/d\Phi_S$ obtained from Eq. (4), we found the expression of the current I_{ds} in accumulation regime:

$$I_{ds}^{acc}=2\pi\Phi_t\mu\frac{R}{L}\left\{C_{ox}\left[\left(V_{geff}+2\Phi_t\right)\Phi_S-\frac{\Phi_S^2}{2}-2\Phi_t\sqrt{\eta}\arctan\left(\frac{\Phi_S-V_{geff}}{\sqrt{\eta}}\right)\right]+Q_{dep}V\right\}_S^D \tag{8}$$

where S and D denote the limits at the source $\Phi_S(0)$ and the drain $\Phi_S(L)$, respectively.

Similarly, by calculating the integral in Eq. (6) based on $dV/d\Phi_S$ derived from Eq. (5) when the device is biased on partly depleted regime, then we obtained the following expression of the current I_{ds} in partly depleted regime:

$$I_{ds}^{par}=2\pi\Phi_t\mu\frac{R}{L}\times\left\{C_{ox}\left[\left(\Phi_S-V_{geff}-\Phi_t\right)\Phi_t\exp\left(\frac{\Phi_S-V}{\Phi_t}\right)+i_c^p+\left(\delta-\beta V_{geff}\right)\frac{V_{geff}}{4}+\frac{3\delta^2}{16\beta}\right]+Q_{dep}V\right\}_S^D \tag{9}$$

where S and D denote the limits at the source $\Phi_S(0)$ and the drain $\Phi_S(L)$, respectively.

A simple interpolation function based on the square root of the algebraic sum of Eq. (7) and Eq. (9) for a continuous

solution of I_{ds} current in depletion regime $I_{ds}^{dep} = \left(\left(I_{ds}^{sub}\right)^2 + \left(I_{ds}^{par}\right)^2 \right)^{1/2}$. In the case of accumulation regime we use the explicit analytical solution of Eq. (8).

3 Results and Discussions

For the validation of the proposed model, the 3-D numerical simulation of the junctionless nanowire (JLN) GAA MOSFET shown in Fig. 1 was carried out with ATLAS tool from SILVACO-TCAD [37], this for the validation of the developed model in the research work that has been implemented in Verilog-A language using SMASH [38]. In this research work, we have considered only for N-type doping structure having the channel radius R and also the body doping concentration N_d at the same time.

Figure 2a-b illustrates respectively the I_{ds}-V_{gs} curves and the Semilog I_{ds}-V_{gs} curves in comparison between the proposed model implemented in Verilog-A (in lines) using SMASH and ATLAS simulation results (symbols) with varying the body doping concentration N_d from 1.0×10^{19} cm^{-3} to 2.0×10^{19} cm^3. Also, the drain bias V_{ds} is set to be 50 mV and the gate bias ranges from 0 to 2 V. The obtained results show that our model implemented in Verilog-A matches well with TCAD simulation results for different body doping concentration N_d. This indicates the accuracy of developed model with standard device with simulation process.

In Fig. 3a-b, we have validated of developed model for the channel radius R, 4.0 nm, 5.0 nm and 6.0 nm respectively. The developed model schematic shown in Fig. 1, implemented in Verilog-A (in lines) presents good agreement with the ATLAS simulation results (symbols). For high values of input voltage shows slight mismatching in between Verilog-A and TCAD simulation results. This indicates accuracy of proposed.

In this section we have observed the impact of device design parameters R and N_d on switching behaviors I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio. From Figs. 2 and 3 it has been observed that, the drain-current variation is strongly influenced by the body doping concentrations N_d and the channel radius R, respectively. It has been also observed that by increasing both N_d and R parameter causes an increase in the variation of the drain-current, especially in the accumulation region. However, the effect of varying the channel radius is more important than the body doping concentrations as shown in Table 1 by means of the ON-current I_{ON}, the OFF-current I_{OFF} and the I_{ON}/I_{OFF} ratio. In addition, the proposed model that has been implemented in Verilog-A predicts well the influence of the channel radius and the doping concentration with a good accuracy and excellent agreement comparing with the TCAD simulation results.

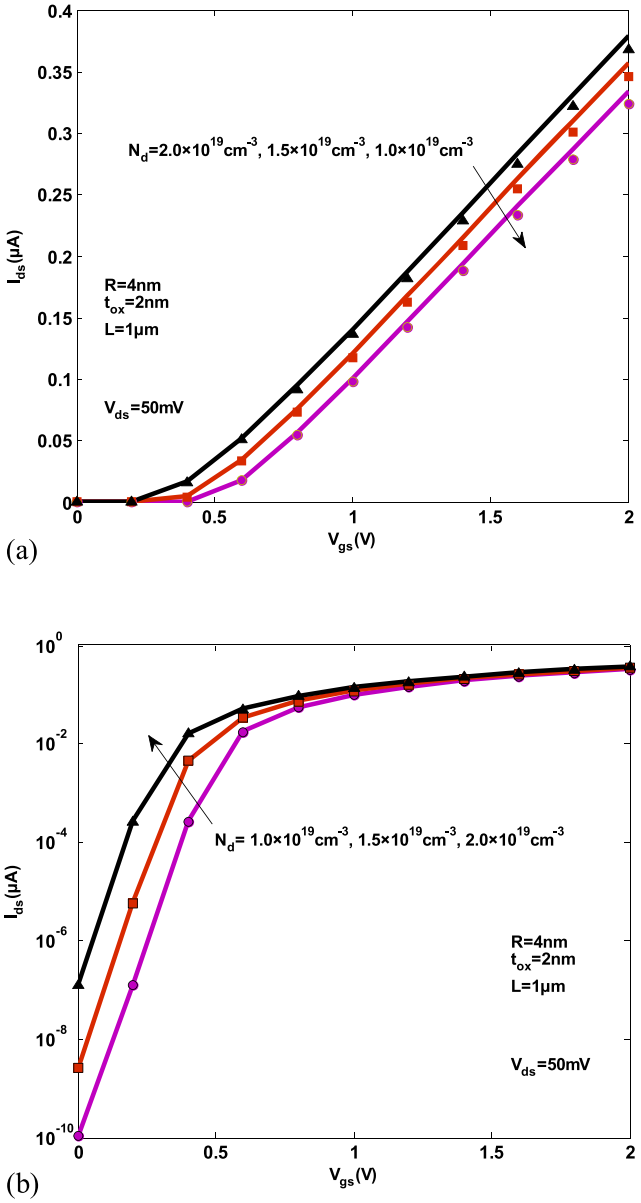

Fig. 2 Transfer characteristics by the Verilog-A model (in lines) compared with TCAD simulation (in Symbols): **a** I_{ds}-V_{gs} curves and **b** Semilog I_{ds}-V_{gs} curves, with varying the doping concentration N_d

In addition, the proposed model that has been implemented in Verilog-A predicts well the influence of the channel radius and the doping concentration with a good accuracy and excellent agreement comparing with the TCAD simulation results.

On the other hand, we have tested the reliability of our model implemented in Verilog-A using SMASH in four types of low voltage circuits: CMOS inverter (Fig. 4a), CMOS NOR-Gate (Fig. 4b), an amplifier (Fig. 5a) and a Colpitts oscillator (Fig. 5b) [39–41].

We have observed in Fig. 6 the good behavior of the voltage transfer characteristic of the inverter obtained through a

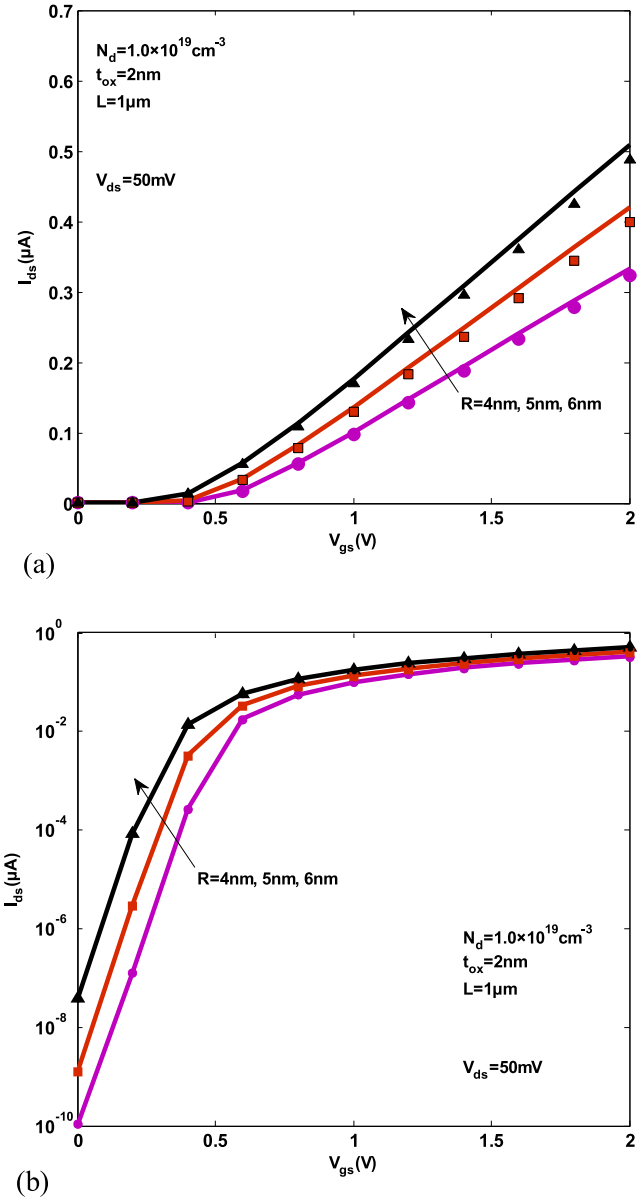

Fig. 3 Transfer characteristics by the Verilog-A model (in lines) compared with TCAD simulation (in Symbols): **a** I_{ds}-V_{gs} curves and **b** Semilog I_{ds}-V_{gs} curves, with varying the channel radius R

Table 1 Extracted parameters of JLN GAA MOSFET

Channel radius (nm)	Body doping concentration (cm^{-3})	I_{ON} (μA)	I_{OFF} (μA)	I_{ON}/ I_{OFF} ratio
4.0	1.0×10^{19} cm^{-3}	0.3337	1.07×10^{-10}	3.11×10^{9}
4.0	1.5×10^{19} cm^{-3}	0.3572	2.57×10^{-9}	1.38×10^{8}
4.0	2.0×10^{19} cm^{-3}	0.3794	1.26×10^{-7}	3.01×10^{6}
5.0	1.0×10^{19} cm^{-3}	0.4196	1.23×10^{-9}	3.41×10^{8}
6.0	1.0×10^{19} cm^{-3}	0.5087	3.91×10^{-8}	1.30×10^{7}

DC simulation with varying the input voltage V_{in} from 0 to 0.8 V, and considering a body radius of 4 nm, an oxide thickness of 2 nm, a channel length of 1 μm and a doping concentration of 1.0×10^{19} cm^{-3}.

The noise margins are usually described by the low noise margin $V_{NML} = V_{IL}$-V_{OL} and the high noise margin V_{NMH}=V_{OH}-V_{IH} [42], where V_{IL} is the low input voltage, V_{OL} is the low output voltage, V_{IH} is the high input voltage and V_{OH} is the high output voltage. Next, we extract the parameter value of V_{IL}, V_{OL}, V_{OH} and V_{IH} from the voltage transfer characteristic of the inverter as shown in Fig. 6. Finally, we calculate the low noise margin as V_{NML} = 0.34 V and the high noise margin as V_{NMH} = 0.32 V. Hence, we found that low noise margin represent 42% of the supply voltage (V_{dd}) and the high noise margin represent 40% of V_{dd}, which provide an excellent stability for the proposed inverter.

Figure 7 shows the transient simulation of the incorporated inverter, we can see the correct behavior of the output voltage V_{out} (against time in "ns") comparing with the input voltage variation V_{in} against time (in line).

By considering a rectangular input waveform as shown in Fig. 7, the average propagation delay t_P can be written as $t_P = (t_{PLH} + t_{PHL})/2$ [42], where t_{PLH} is the low to high propagation and t_{PHL} is the high to low propagation delay. Then, we extract the parameter value of t_{PLH} and t_{PHL} from the inverter output signal as shown on Fig. 7. In addition, we calculate the average propagation delay as t_P = 0.5 ns. The obtained value of average propagation delay is very small which proves the fast response of the incorporated inverter.

Moreover, theoretically the power dissipation of the inverter can be defined as the algebraic sum of the static power dissipation P_{DC}=$I_{dsub}V_{dd}$ and the dynamic power dissipation P_{AC}=P_{swit} + P_{sc} [42, 43], where I_{dsub} is the subthreshold current, P_{swit} is the switching power dissipation and P_{sc} is the short-circuit power dissipation.

The simplified equation of the switching power dissipation is $P_{swit} = fC_LV^2_{dd}$, where f corresponds to the signal frequency and C_L is the load capacitance. Also, the short-circuit power is given by $P_{sc} = (f\tau K(V_{dd}\text{-}2V_{th})^3)/12$ [44], with V_{th} correspond to the device's threshold voltage and K is the transconductance parameter. For symmetrical case the parameter τ is equal to the low to high propagation delay t_{PLH} (and equal to the t_{PHL} parameter) [45, 46].

Based on the above definition, we have calculated the power dissipation of the proposed inverter as 0.0121 mW with a loaded capacitance of 1 pF. It has been observed that the inverter power dissipation is strongly dominated by the switching power dissipation P_{swit} because of P_{sc} < 10 × P_{swit} and the very low leakage-current based the considered parameter of the transistors and the elimination of P/N (and N/P) junction in the case of junctionless device.

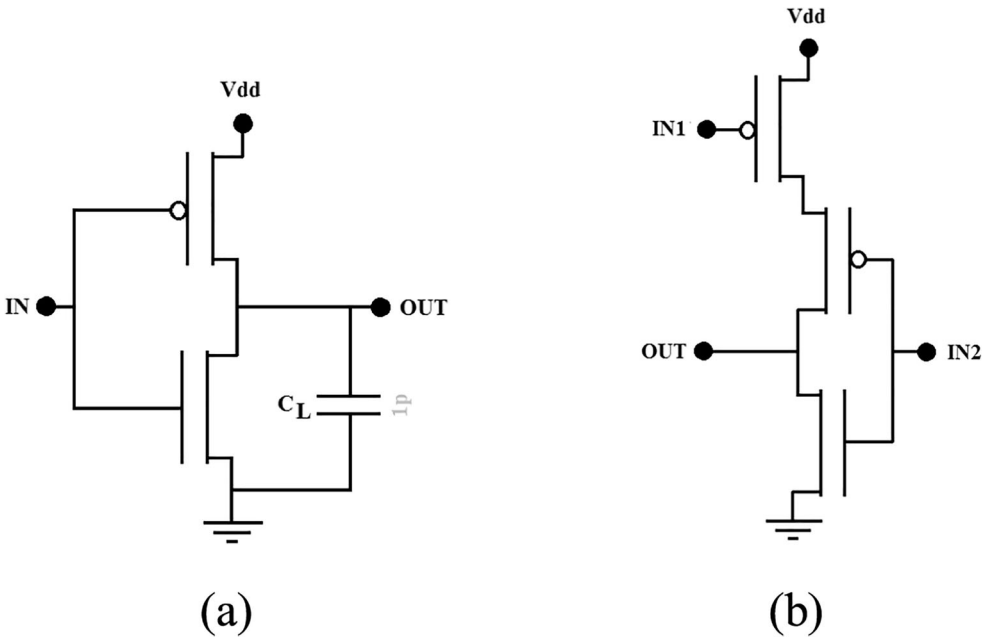

Fig. 4 **a** Circuit diagram of the implemented CMOS inverter. **b** Circuit diagram of the implemented CMOS NOR-Gate

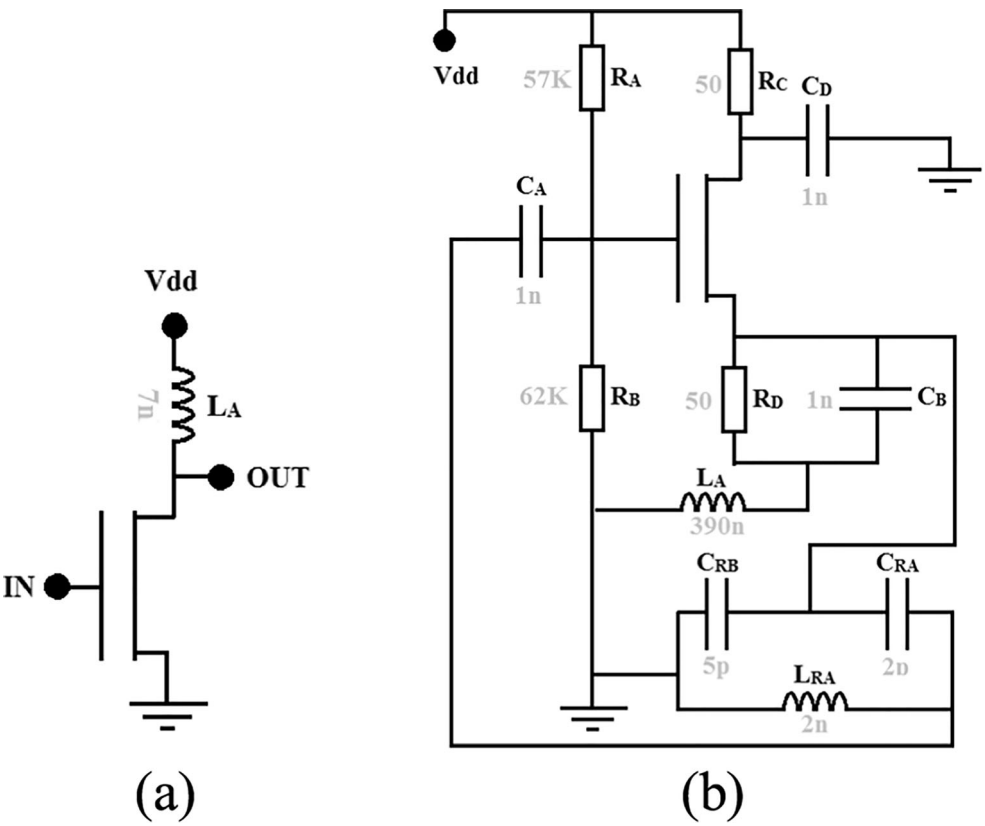

Fig. 5 **a** Circuit diagram of the implemented amplifier. **b** Circuit diagram of the implemented Colpitts oscillator

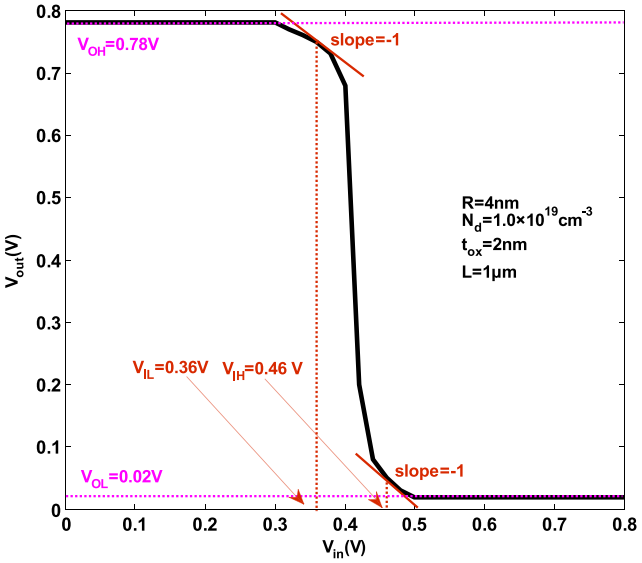

Fig. 6 Voltage transfer characteristic of the implemented inverter using SMASH, where V_{in} is the input voltage and V_{out} is the output voltage

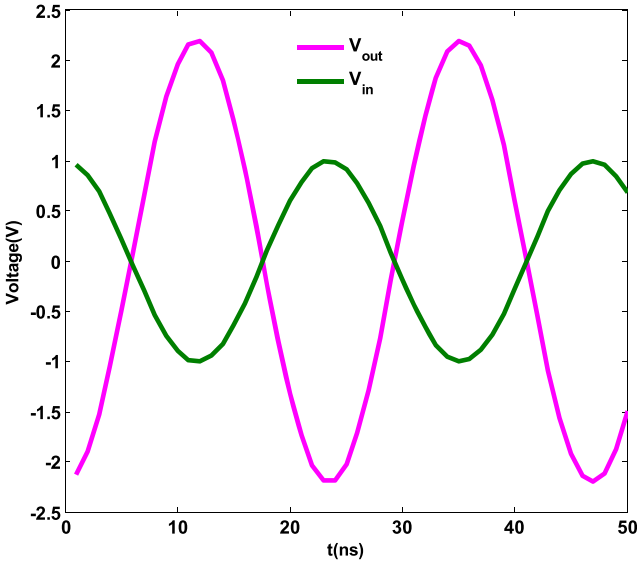

Fig. 8 Transient simulation of the implemented amplifier using SMASH, where V_{in} is the input voltage and V_{out} is the output voltage. R = 4 nm, t_{ox} = 2 nm, L = 1 μm and $N_d = 1.0 \times 10^{19}$ cm^{-3}

Figure 8 shows the transient simulation of the incorporated amplifier, we can see the accurate behavior of the output voltage V_{out} (against time in "ns") with respect to the applied input voltage variation V_{in} against time. Based on the devise's parameter (R = 4 nm, t_{ox} = 2 nm, L = 1 μm and $N_d = 1.0 \times 10^{19}$ cm^{-3}) and the considered value of the inductor we have optimized the Gain of incorporated circuits (≈ 2.2).

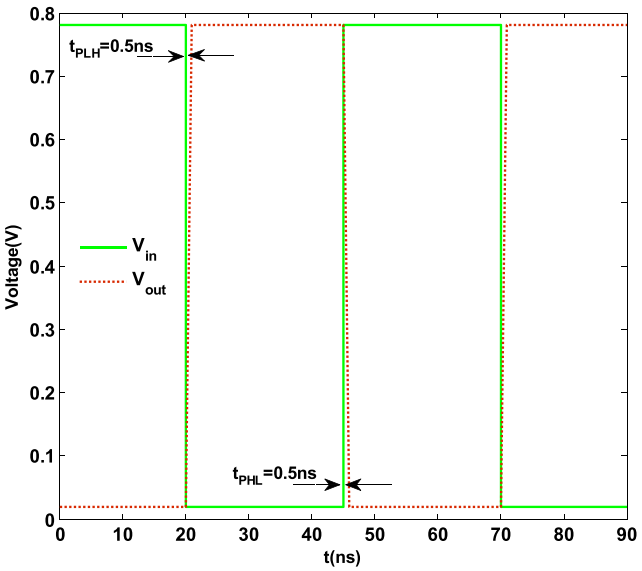

Fig. 7 Transient simulation of the implemented inverter using SMASH, where V_{in} is the input voltage and V_{out} is the output voltage. R = 4 nm, t_{ox} = 2 nm, L = 1 μm and $N_d = 1.0 \times 10^{19}$ cm^{-3}

The transient simulation of the CMOS NOR-Gate is well presented in Fig. 9. The applied input voltage are shown in Fig. 9a, where V_{in1},V_{in2} are the first and the second input voltage, respectively. As expected, the output voltage showed in Fig. 9a reproduce well the logic operation of the incorporated NOR-Gate.

Figure 10 illustrates the transient simulation of the Colpitts oscillator with a JLNGAA MOSFET, we can see the good electrical behavior and the excellent stability of the generated oscillation of the output voltage variation V_{out} versus time (segmented lines), with considering a body radius of 4 nm, an oxide thickness of 2 nm, a channel length of 1 μm and a doping concentration of 1.0×10^{19} cm^{-3}.

The good and accurate results of the transient and DC simulations of the inverter and the Colpitts oscillator based on JLNGAA MOSFET using SMASH proves the validity of the model implemented in Verilog-A and also its reliability for circuits simulation as well.

4 Conclusion

In conclusion, we have developed a compact model having no fittings parameters with less analytical complex formulation-based physics-based concept. This indicates better accuracy with lesser complexity. The developed analytical compact model for junctionless nanowire GAA MOSFET verified in Verilog-A using SMASH circuit simulator technique. The accuracy of developed compact model has been validated using TCAD simulation results with varying the doping concentration (N_d) and

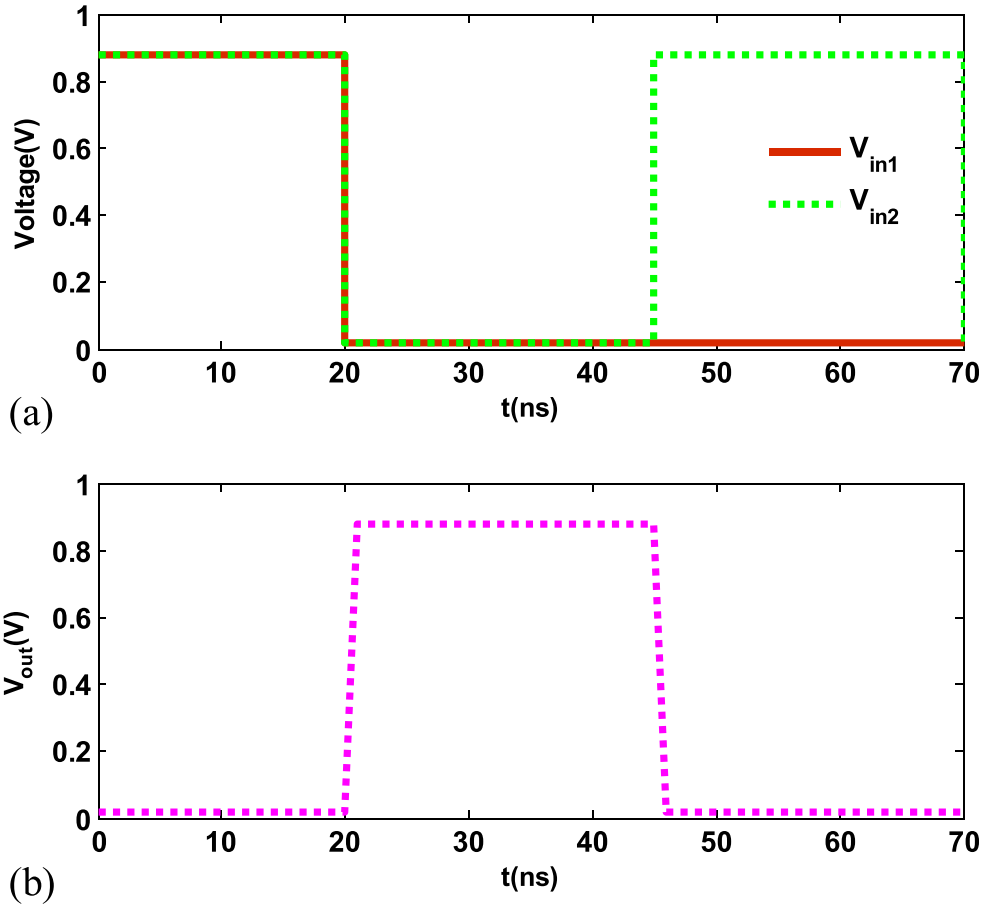

Fig. 9 Transient simulation of the implemented CMOS NOR-Gate with SMASH. **a** Applied input voltage. **b** Obtained output voltage. R = 4 nm, t_{ox} = 2 nm, L = 1 μm and N_d = 1.0 × 10^{19} cm^{-3}

the channel radius (R) of the transistor. In this context, the comparison between the Verilog-A model results and the simulations results show excellent agreement and a good accuracy of the current-voltages (I_{ds}-V_{gs}) model. Finally, for the first time, we have tested the JLNGAA MOSFET model in Verilog-A language for both digital and analog circuits. The correct results of DC and transient simulations of the incorporated circuits prove the validity of the model in Verilog-A and also its reliability for digital and analog circuit simulation.

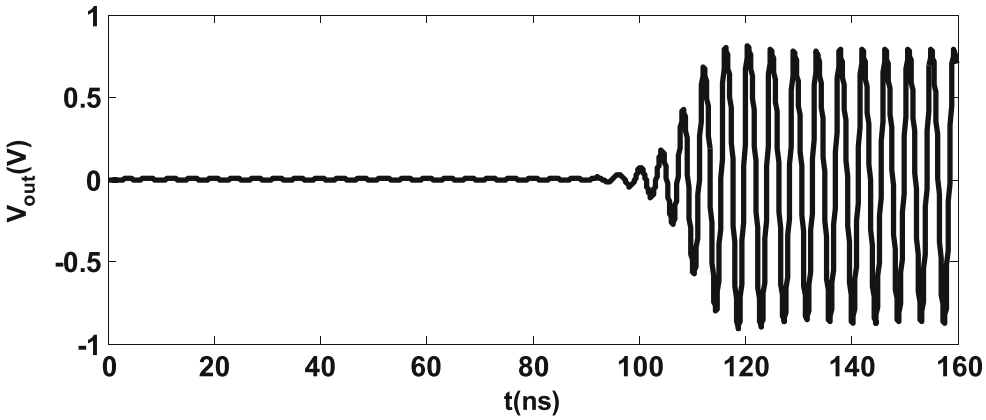

Fig. 10 Transient simulation of the implemented Colpitts oscillator using SMASH, where V_{out} is the output voltage. R = 4 nm, t_{ox} = 2 nm, L = 1 μm and N_d = 1.0 × 10^{19} cm^{-3}

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