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Design and analysis of novel La:HfO_2 gate stacked ferroelectric tunnel FET for non-volatile memory applications

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ABSTRACT

Recent experimental studies have shown lanthanum-doped hafnium oxide (La:HfO_2) possessing ferroelectric properties. This material is of special interest since it is based on lead-free, simple binary oxide of HfO_2, and has excellent endurance property (1×10^9 field cycles without fatigue. There exists substantial information about the material aspects of La:HfO_2 but it lacks proven application potential for CMOS-compatible low-power memory design. In this work, 10 % La metal cation fraction of HfO_2 (La:HfO_2) is proposed as the gate stack material in tunnel FET (TFET) for its potential as a memory device. 2D device simulations are carried out to show that the proposed ferroelectric TFET (FeTFET) provides the largest memory window (MW) as compared to present perovskite ferroelectric materials such as PZT, SBT ($SrBi_2Ta_2O_9$) and silicon doped (4.6 % Si in HfO_2) hafnium oxide (Si:HfO_2). The larger window is attributed to greater polarization, and the calculation of MW is quantified by the shift in threshold voltage (V_{th}). The simulations carried out in this work suggest that La:HfO_2 can be adopted as a potential ferroelectric material to target low-power FeTFET design at significantly reduced ferroelectric layer thickness.

1. Introduction

Immense research on TFETs has been done so far, which points towards their suitability as an alternative to conventional MOSFETs since they are expected to surmount the fundamental shortcomings of MOSFETs by employing the concept of band-to-band tunneling of charge carriers [1–7]. TFET allows a more significant reduction in supply voltages with reduced power consumption. Integrating the ferroelectric gate stack with TFETs has attracted researchers' interest in the memory applications domain. Dynamic Random Access Memories (DRAMs) and Flash memories are being used hand in hand as one provides speed and the other provides non-volatile functionality. Modern-day electronics require non-volatile memories having a compact size, low power consumption, and faster speed. In this regard, ferroelectric materials are being explored as an energy-efficient compact-sized alternative to existing non-volatile memories [8–18]. Data storage and retention in ferroelectric-based memories is achieved owing to the hysteresis property of the ferroelectric materials, which is controlled by the applied electric field [19–22]. The most commonly used ferroelectric materials faced severe limitations in terms of high leakage currents, time-dependent breakdown over repeated cycles of use, and scaling capabilities as they required large ferroelectric layer thickness to get the necessary MW. Si:HfO_2 is one of the most promising ferroelectric layer candidates right now since it provides a large MW with the additional advantage of CMOS compatibility [23]. Ferroelectric-based TFETs have a huge potential to be used as non-volatile memory with a significantly large MW. TFET's (shown in Fig. 1) working principle is quantum tunneling of the charge carriers through the barrier contrary to the classical mechanism of thermionic emission of charge carriers over the barrier. When a positive voltage is applied on the gate of TFET, the energy bands of the channel bend downward and electrons from the valence band of the P-type source tunnel into the conduction band of the

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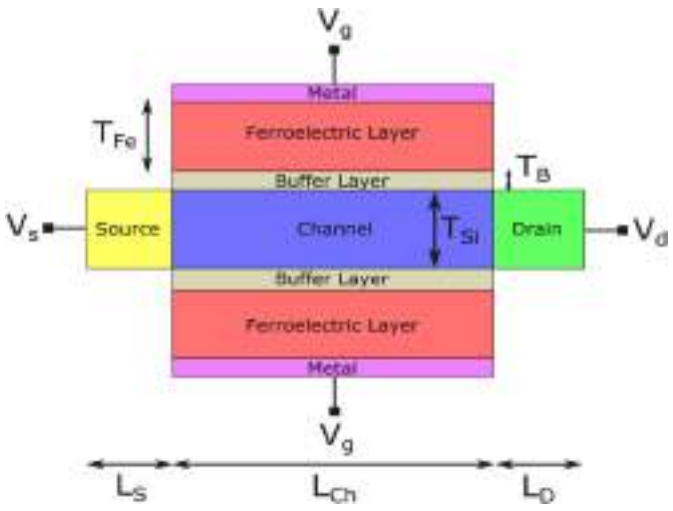

Fig. 1. Device design of La:HfO_2 FeTFET.

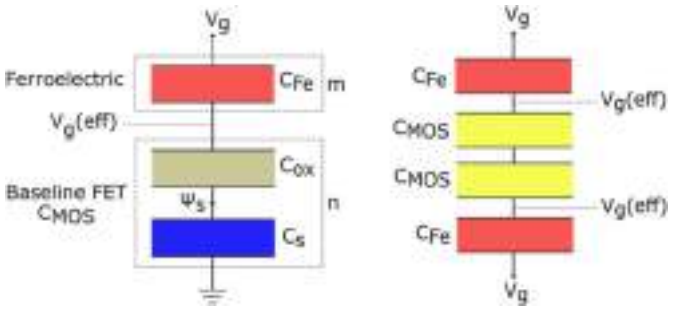

Fig. 2. Simplified capacitance model of the proposed device.

Table 1
Ferroelectric property values of currently used ferroelectric materials [23, 32–35].

Material	P_r (μC/cm^2)	E_c (MV/cm)	ε_r
SBT	8	0.08	250
PZT	32	0.26	250
Si:HfO_2	9	1.1	32
La:HfO_2	27.7	1.4	26

Table 2
Device simulation parameters.

Parameter	Symbol	Value
Source Doping (Boron) (cm^{-3})	N_S	1×10^{20}
Channel Doping (Arsenic) (cm^{-3})	N_{Ch}	1×10^{16}
Drain Doping (Arsenic) (cm^{-3})	N_D	1×10^{18}
Source Length (nm)	L_S	4
Channel Length (nm)	L_{Ch}	28
Drain Length (nm)	L_D	4
Silicon Body Thickness (nm)	T_{Si}	10
Buffer Layer Thickness (nm)	T_B	1
Ferroelectric Layer Thickness (nm)	T_{Fe}	10

n-type channel which allows the flow of current in the device. TFETs have the inherent property of low power consumption, faster switching speed and provide non-volatile data storage at a smaller chip size, thus making them cost-effective. Combining these two technologies is expected to give excellent outcomes in terms of cost and power-efficient devices at reduced sizes. Implementing a novel ferroelectric material with higher polarization will provide an additional boost to the device's performance. As per the findings [24–28], the dopants with the greatest impact on stabilizing the ferroelectric non-centrosymmetric orthorhombic phase in hafnium oxide are the lanthanide series elements, in addition to Ca, Sr, and Ba. Among the well-explored hafnia-based ferroelectric films outlined till now, La:HfO_2 is showing the highest remanent polarization (P_r) value, excellent endurance (1×10^9 field cycles without fatigue), and compatibility with CMOS back-end at lower La concentrations [29].

The MW is the most crucial parameter in non-volatile memory devices, which is the amount of variation (in volts) between the threshold voltages of the two polarization curves of the device. Large MW renders large retention time, and data detection becomes easy in non-volatile memory. The data gets stored in the channel between the source and drain when the gate voltage is applied through the word line. When the voltage is withdrawn, the data is retained since the induced remnant polarization continues to hold the channel charge. The channel current can be used to sense the data on the transistor. So, this work focuses on the effects of using La:HfO_2 as ferroelectric gate stack material on the MW of the device (La:HfO_2 FeTFET), and analyzing the influence of buffer layer material on the device performance. To prevent the interdiffusion or reaction causing charge trapping, a buffer layer is placed between the ferroelectric material and the silicon channel. A Ferroelectric MOSFET (FeMOSFET) using La:HfO_2 as gate stack material is simulated as well and compared with FeTFET keeping all parameters the same for both devices.

2. Device Design

The 2-Dimensional schematic of 28 nm gate length silicon n-channel double gate FeTFET is shown in Fig. 1. V_g, V_s, and V_d represent the gate voltage, source voltage, and drain voltage, respectively. T_{Fe}, T_B, T_{Si}, L_S, L_{Ch}, and L_D represents the ferroelectric layer thickness, buffer layer thickness, silicon body thickness, source length, channel length, and drain length, respectively. The 28 nm technology node is a half-node semiconductor manufacturing process used as a stop-gap between the 32 nm and 22 nm processes. Although lower technology nodes are being explored, short channel effects (SCEs) become aggravated at lower tech-nodes, and reliable lithography becomes challenging. In addition, when it comes to buffer layer, 1-nm HfO_2 buffer layer is considered, since recent epitaxy process can deposit 0.1 nm HfO_2 layer per 1 cycle. This structure is designed with the condition that the HfO_2 buffer layer could be grown through 10 epitaxy cycles. The proposed device would require additional analysis of SCEs if the gate length is smaller than 28 nm.

Fig. 2 displays a simplified representation of the capacitances pertaining to the gate stack of the proposed device. One of the most attractive properties of ferroelectric material is negative capacitance (NC). This property allows the material to behave as a voltage step-up transformer, improving the device's subthreshold-swing (SS) and drain current. The condition for stability of negative capacitance is given as follows in eqs. (1) and (2):

$$\frac{1}{C_{total}} = \frac{1}{C_{MOS}} + \frac{1}{|C_{Fe}|} > 0 \tag{1}$$

$$\Rightarrow |C_{Fe}| > C_{MOS} \tag{2}$$

where, C_{Fe}, C_{MOS}, and C_{Total} denote ferroelectric, baseline MOS and total capacitances [30].

The crucial point to note here is that the $C_{Fe} < 0$, as the P-E (Q-V) curve slope is negative (hence the name negative capacitance) and $C_{Total} > C_{MOS}$. The baseline MOS structure acts as the dielectric, which can stabilize the ferroelectric's negative capacitance state, and hysteretic behavior will be observed if this condition is violated [31].

The doping concentration in the source, channel, and drain region is 10^{20} atoms/cm^3 of boron material, 10^{16} atoms/cm^3 arsenic, and 10^{18} atoms/cm^3 arsenic, respectively. 10 nm thick La:HfO_2, having a lanthanum dopant concentration of 10 % is used as the ferroelectric

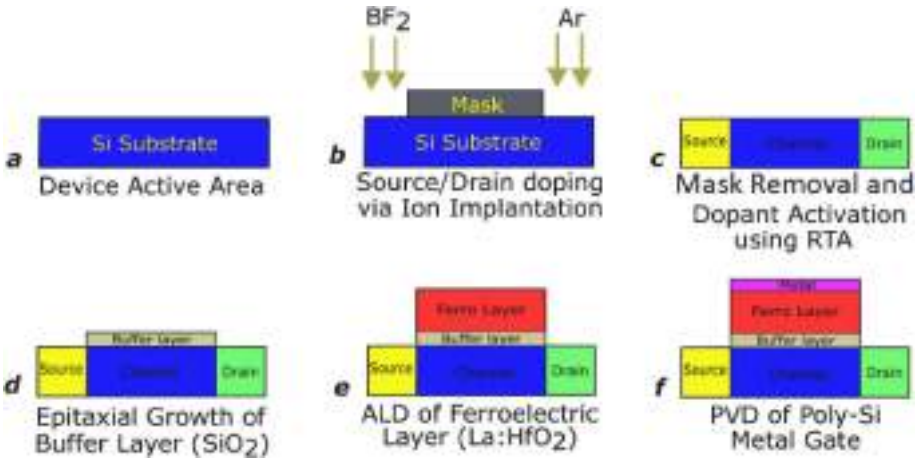

Fig. 3. Fabrication steps to achieve the suggested La:HfO_2 FeTFET.

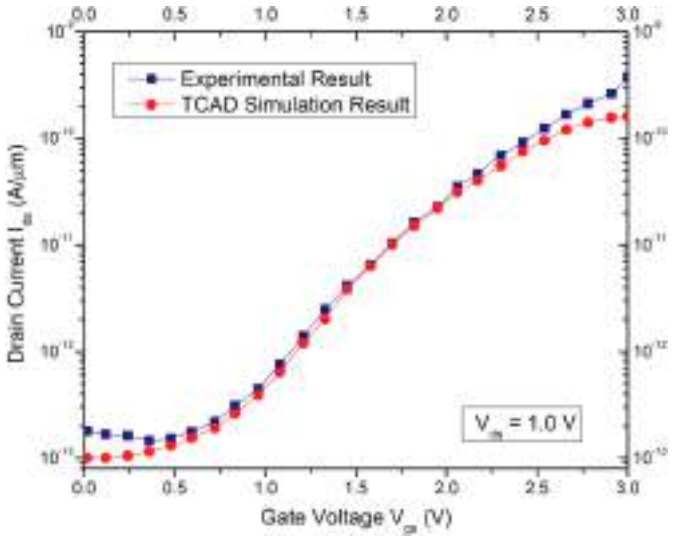

Fig. 4. Caliberated transfer characteristics of the proposed device with the experimental data (NC-TFET) [35].

layer in this work. It has 27.7 μC/cm^2 remanent polarization, 1.4 MV/cm coercive field (E_c), and relative permittivity value 26 [32]. Table 1 lists the remanent polarization, coercive field, and permittivity at 10 nm ferroelectric layer thickness used in this study. Table 2 lists the design simulation specifications of the proposed device.

3. Fabrication process flow and model validation

In terms of the practical possibility of implementing the suggested device that involves creating a La:HfO_2 thin film, Fig. 3 depicts the consecutive stages entailed in its fabrication process. Silicon wafer cleaning is performed as the first step to achieve the desired device

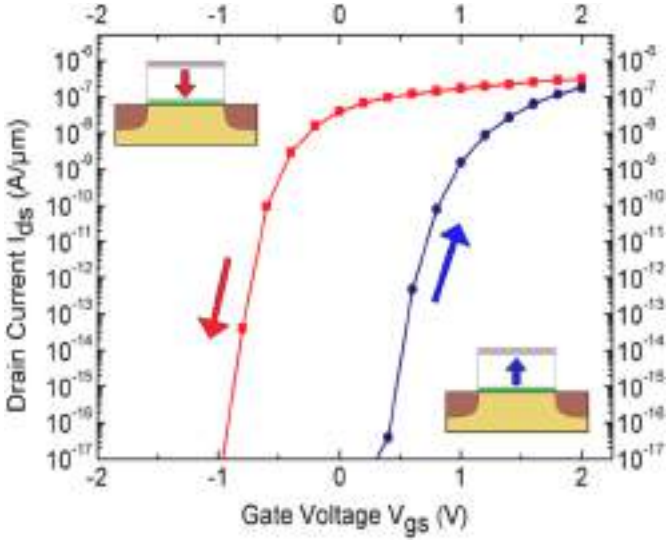

Fig. 6. I_{ds} vs. V_{gs} characteristics of the proposed device at V_{ds} = 0.5 V.

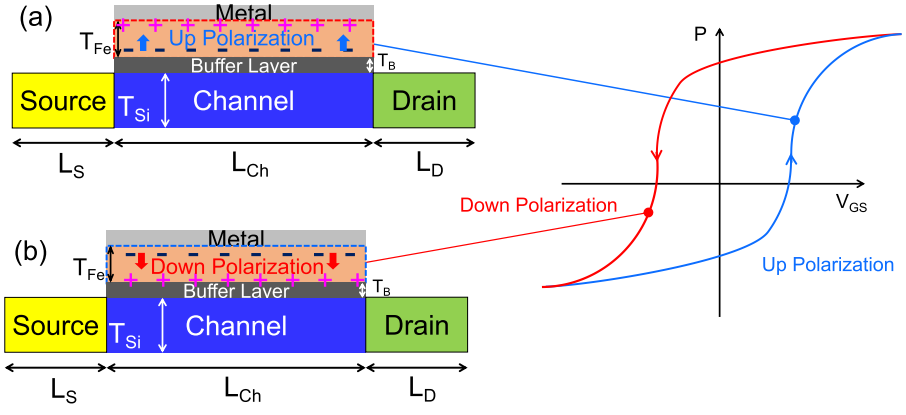

Fig. 5. Polarization phenomena of the proposed device.

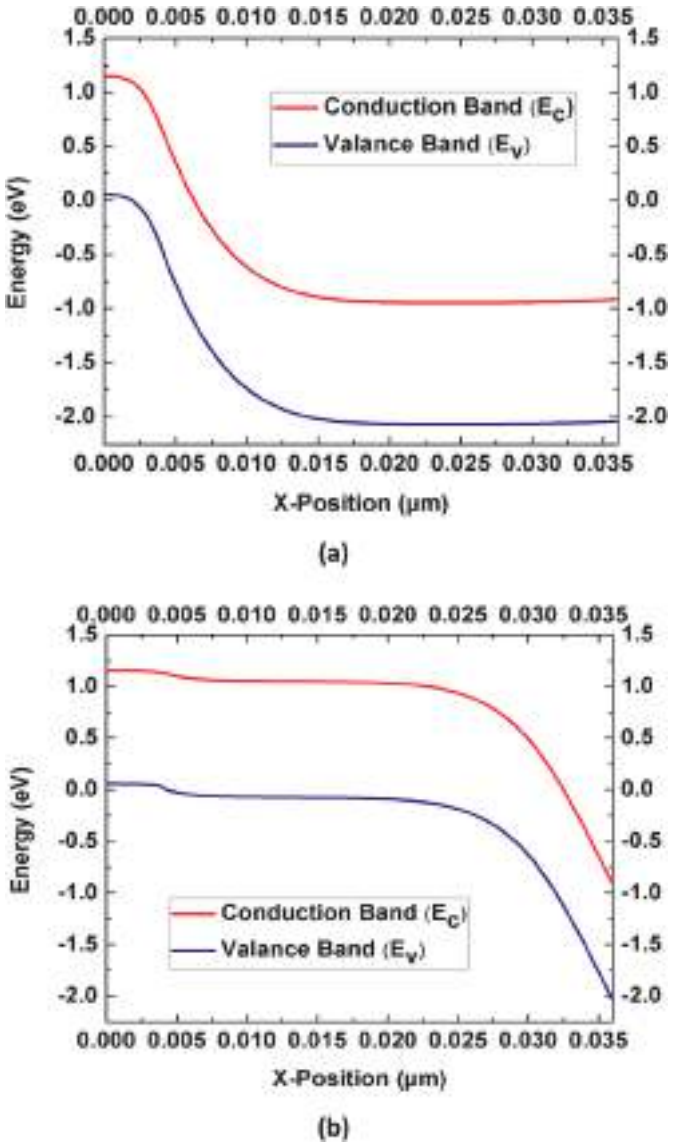

Fig. 7. Band Diagram of proposed device at V_{gs} sweep of (a) −2 to 2 V (Forward) and (b) 2 to −2 V (Reverse) at V_{gs} = 0.5 V.

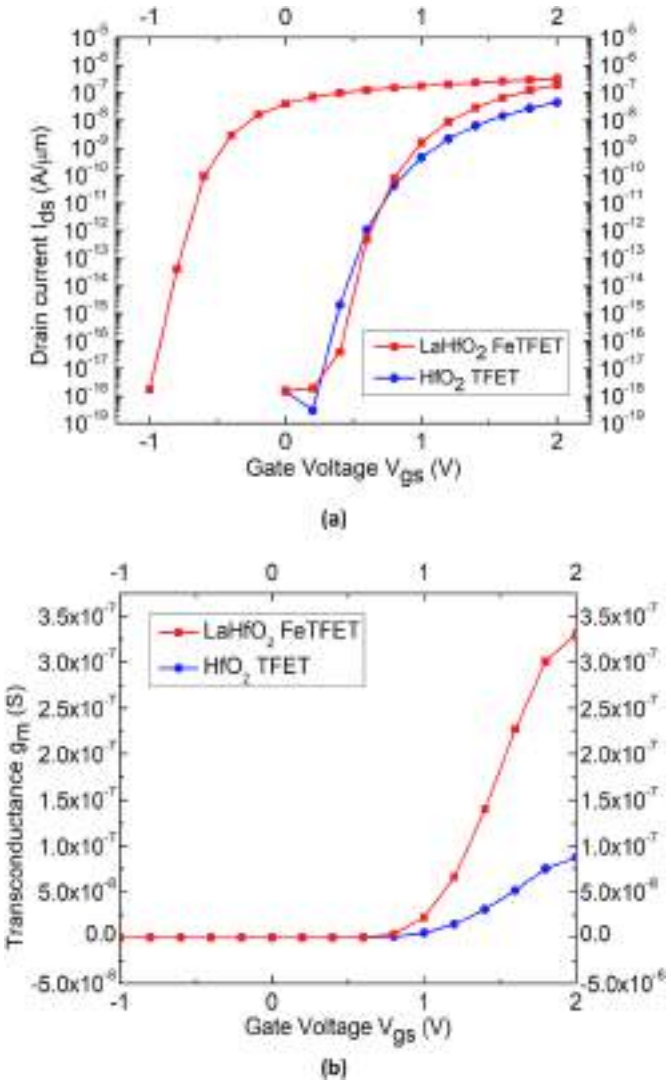

Fig. 8. (a) Transfer characteristics of the proposed FeTFET and conventional HfO_2 TFET at V_{ds} = 0.5 V and (b) Transconductance (g_m) curve of proposed FeTFET and conventional HfO_2 TFET at V_{ds} = 0.5 V.

(Fig. 3(a)). Then, the field oxide is deposited, out of which the FET active area is etched using an appropriate chemical etchant such as buffered oxide or hydrofluoric acid via photolithography. Arsenic (Ar) and Difluoroboron (BF_2) ions are used to dope the source and drain regions using a CMOS-compatible half mask [36,37] (Fig. 3(b)). After completion of doping, the mask layer is chemically etched and the dopants are activated using rapid thermal annealing process (Fig. 3(c)). The epitaxial buffer layer is then thermally grown [38] as shown in Fig. 3(d). The ferroelectric layer of La:HfO_2 can be grown by the very well mature plasma-assisted Atomic Layer Deposition (ALD) technique with very high conformity [39] (Fig. 3(e)). La:HfO_2 thin films are compatible with CMOS technology and possess the potential to form 3D structures. Thus, they can be conveniently integrated with the TFETs. The last step is polysilicon metal gate formation using physical vapor deposition, metallization, and H2 sintering [36] (Fig. 3(f)).

To simulate the proposed device structure and analyze the results, commercially available 2D TCAD tool Synopsys Sentaurus-Device (S-Device) is used. The tunneling probability is computed using the default WKB-based tunneling model. Among the four available carrier transport models, drift-diffusion is the most appropriate model to be incorporated for the proposed device. To account for the generation and recombinations occurring between the bands, doping dependent SRH Recombination model is implemented. Another critical Non-Local Path BTBT model applied here calculates the generation rate based on the bend bending due to the electric field present in the device. Doping-dependent mobility and effective intrinsic density models accounting for bandgap narrowing are also included. The Ferro model is also enabled with appropriate values of ferroelectric properties of the gate stack material. The selected model parameters of the simulation are calibrated to fit the experimental data [35,40]. As shown in Fig. 4, our simulation result has been compared with the fabricated NC-TFET, which has been widely adopted for low power application [35]. The targeted fabricated NC-TFET has planar structure with silicon (Si) channel, which is similar structure to our proposed structure [35]. Process parameters such as device dimensions and doping concentration is used as a starting point for simulation. Then, reduced mass m_r is used as a fitting parameter to fit the simulated data with the experimental data. The proximity of both curves affirms the accuracy of the chosen models for simulation.

4. Simulation results and discussion

The two polarization curves of La:HfO_2 FeTFET are presented in

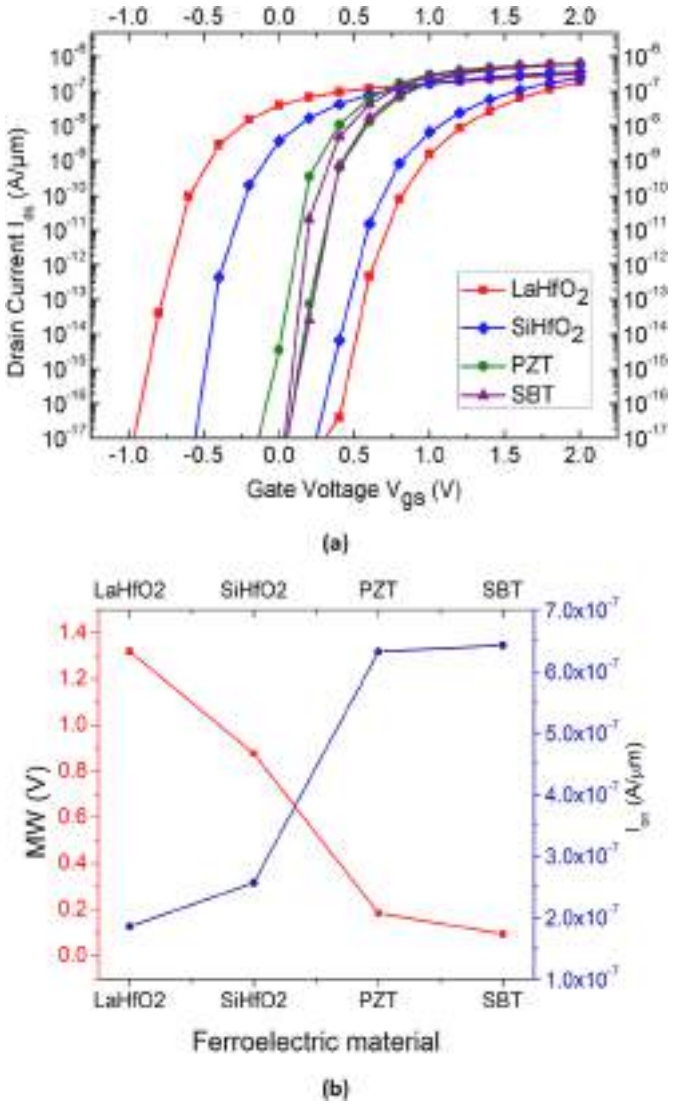

Fig. 9. (a) I_{ds} vs. V_{gs} characteristics of the FeTFET with different ferroelectric layer materials at V_{ds} = 0.5 V and (b) Variation of MW and I_{on} with ferroelectric layer.

Table 3
Theoratical vs. obtained MW at t = 10 nm.

Material	Theoratical maximum MW (V)	This work MW (V)
SBT	0.16	0.095
PZT	0.52	0.185
Si:HfO_2	2.20	0.877
La:HfO_2	2.80	1.320

Fig. 5(a–b). First, the gate is swept from -2 to +2 referred to as the forward sweep, and then back to -2 referred to as the reverse gate voltage sweep. The two curves represented in blue (Fig. 5(a)) and red (Fig. 5(b)) correspond forward and reverse sweep, respectively. These curves show variation in the threshold voltages, which is due to the hysteresis property of the ferroelectric layer (La:HfO_2). The difference between these two threshold voltages is referred to as the MW of the device. The I_{ds} vs. V_{gs} characteristics of La:HfO_2 FeTFET at V_{ds} = 0.5 V is shown in Fig. 6. Until recent times, the voltage that corresponded to the drain current of 10^{-7} A/μm was universally accepted as the threshold voltage of the TFET, but this method holds very little physical significance. This work uses a more precise method for calculating the

Table 4
Comparison of electrical characteristics of proposed device with state-of-the-art [23,47–55].

Reference Work	Material	Ferro layer thickness (nm)	MW (V)	SS (mV/dec)
[23]	Si:HfO_2	10	1.7	–
		15	2.05	
		20	2.3	
[47]	Si:HfO_2	2	0.32	23
		4	0.25	19.6
		6	0.21	17.3
[48]	Si:HfO_2	10	1.8	–
		30	4	
[49]	$HfZrO_x$	15	0.55	–
[50]	$HfZrO_x$	5	1.37	–
[51]	$HfZrO_x$	6	0.3	51
[52]	$HfZrO_x$	11.5	2.5	–
[23]	SBT	230	1.7	–
[53]	SBT	400	1.6	–
[54]	SBT	200	1.81	–
[23]	PZT	50	1.7	–
[55]	PZT	160	2	–
This work	La:HfO_2	10	1.32	28

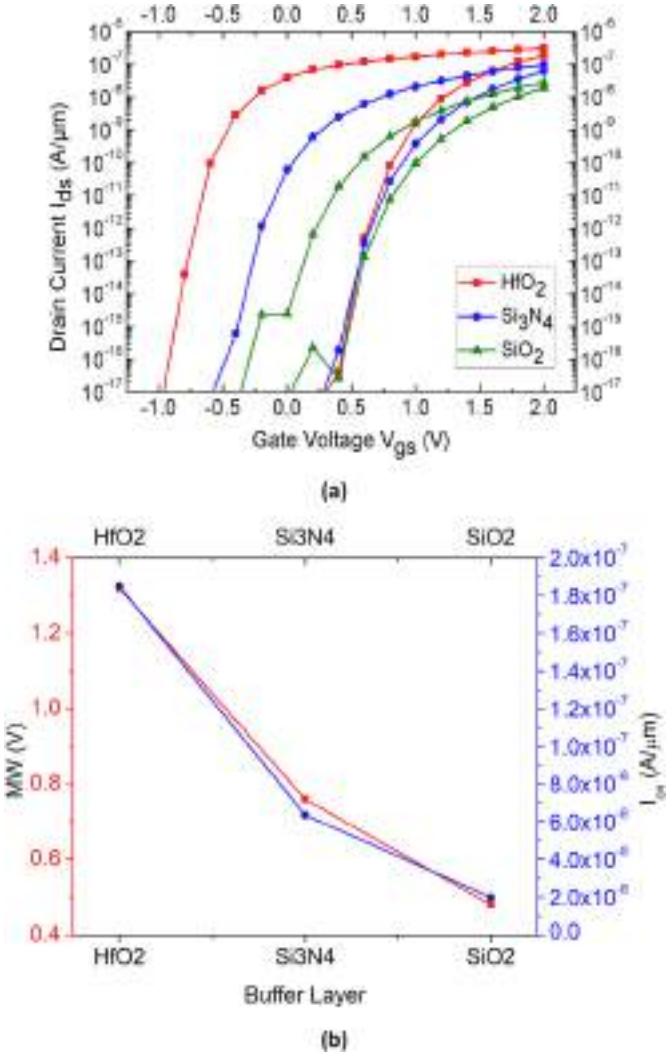

Fig. 10. (a) I_{ds} vs. V_{gs} characteristics of the proposed FeTFET with different buffer layer materials at V_{ds} = 0.5 V and (b) Variation of MW and I_{on} with buffer layer.

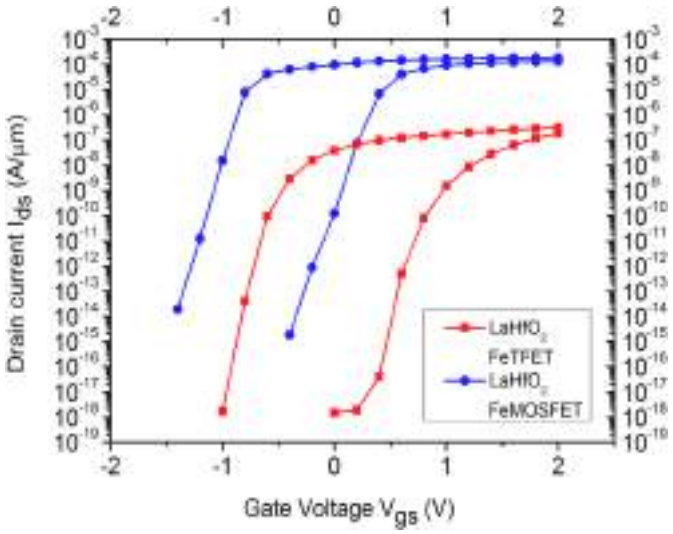

Fig. 11. I_{ds} vs. V_{gs} characteristics of the proposed FeTFET and FeMOSFET at $V_{ds} = 0.5$ V.

Table 5
Electrical parameter value at different variants of the proposed device.

Parameter	Variant	MW (V)	SS (mV/dec)
Ferroelectric Material	La:HfO_2	1.320	28
	Si:HfO_2	0.877	25
	PZT	0.185	18
	SBT	0.095	12
Buffer Material	HfO_2	1.320	28
	Si_3N_4	0.760	33
	SiO_2	0.480	38
FeTFET	La:HfO_2	1.320	28
TFET	HfO_2	–	34
FeMOSFET	La:HfO_2	0.910	36

threshold voltage. V_{th} is directly controlled by the energy barrier width narrowing, which saturates at higher gate voltage [41]. This definition is consistent with the MOSFET threshold voltage as well.

The band diagrams help get finer insights into the working of the proposed FeTFET. The band structure of the proposed device at forward and reverse gate voltage sweep is shown in Fig. 7(a–b). When the gate is swept towards positive voltage, the dipole direction of the ferroelectric material will be towards the channel, and the channel becomes N-type, as shown in Fig. 7(a). This down polarization state corresponds to the "OFF" (0) state having a higher threshold voltage. Now, if we sweep the gate voltage from positive to negative, the dipole direction will turn opposite towards the gate. The channel now becomes P-type as shown in Fig. 7(b). This up polarization state is referred to as the "ON" (1) state with a lower threshold voltage. Any change in P_r is reflected as an increment/decrement in the MW of the device.

In Fig. 8(a), we can observe the comparison between the transfer characteristics of La:HfO_2 FeTFET and conventional HfO_2 dielectric based TFET (HfO_2 TFET) using identical buffer and ferroelectric layer thickness. Ferroelectric transistors exhibit negative capacitance effects other than their ability for data storage. The ferroelectric property of the material creates an internal voltage amplification (A_v) effect, which can be obtained from the equivalent voltage divider circuit as follows in eq. (3):

$$A_v = \frac{C_{Fe}}{C_{Fe} + C_{MOS}} > 1 \; for \; C_{Fe} < 0 \tag{3}$$

The SS of the FeTFET can be calculated as eqs. (4) and (5):

$$SS = \frac{\partial V_{gs}}{\partial log_{10} I_{ds}} = \frac{\partial V_{gs}}{\partial V_{MOS}} \frac{\partial V_{MOS}}{\partial \psi_s} \frac{\partial \psi_s}{\partial log_{10} I_{ds}} \tag{4}$$

$$= \frac{1}{A_v m} \frac{\partial \psi_s}{\partial log_{10} I_{ds}} = \frac{1}{A_v m} . n \tag{5}$$

where, m is the body factor of internal FET, n is the transport factor and ψ_s is the surface potential. The transport factor gives the value 60 mV/dec at room temperature in the subthreshold region. Thus, the amplification A_v due to negative capacitance effect reduces SS below Boltzmann limit if A_v. $m > 1$. Such voltage gain not only reduces the SS of the device but also boosts the channel charge density in the region of inversion due to which a larger ON current is achieved in comparison to the HfO_2 TFET [42–44].

As seen from Fig. 8(a), the ON current of proposed La:HfO_2 FeTFET is 1.85×10^{-7} A/μm whereas it is 4.4×10^{-8} A/μm in the case of conventional HfO_2 TFET. The variation of transconductance with gate voltage V_{gs} is shown in Fig. 8(b) g_m is formulated as $(\partial I_{ds} / \partial V_{gs})$. It depicts the amplification capability of the device. In other words, devices with a higher value of g_m convert input voltage to output current better than those with low gm. g_m of the proposed device is 3.31×10^{-7} S whereas it is 8.735×10^{-8} S in the case of conventional TFET. Thus, the ON current and transconductance achieved in the case of La:HfO_2 FeTFET is 4 times higher than the conventional TFET. The SS of La:HfO_2 FeTFET is 28 mV/dec. whereas it is 34 mV/dec in case of HfO_2 TFET, which is 18 % less than the conventional TFET. This improvement in the performance of La:HfO_2 FeTFET is due to the reasons stated eq. (3). Achieving high ON current at very low supply voltage can be made possible with devices having low SS thus enabling the supply voltage scaling targets.

To compare proposed La:HfO_2 based FeTFET with existing ferroelectric gate stack materials currently being used in memory devices such as PZT, SBT, and Si:HfO_2, all the design parameters were kept the same. Ferroelectric and buffer layer thicknesses used for all the four devices are 10 nm and 1 nm, respectively.

As seen from Fig. 9(a), La:HfO_2 provides the largest MW among Si:HfO_2, PZT, and SBT. This result is mainly obtained due to the higher coercive field of La:HfO_2 compared to others. The coercive field is defined as the field that causes the polarization direction to switch. The two directions of polarization in the ferroelectric material separate the V_{th} of the two states of the device i.e. "ON" and "OFF". This means that a

Table 6
Comparison among the three FETs [57].

Performance Parameter	TFET	Fe-TFET	Fe-FET
Electrical Parameters	SS: >60mV/dec MW: NA	SS: 10 mV/dec. MW: 48 mV	SS: >40mV/dec. MW: 12 mV
Working Principle	The BTBT concept is used to enhance the device performance by improving (body, and transport) factors at the same time.	The NC and BTBT concepts are simultaneously used to boost the device performance by optimizing body and transport factors at the same time.	The NC concept is used to boost the device performance by optimizing body and transport factor.
Fabrication	Similar to the CMOS fabrication; only structural difference lies in the opposite doping of the TFET source and drain.	The FE layer integrated into the gate stack by the lithography pattern and deposited by an electron beam evaporator and lift-off process.	FeTFET produced in a manner akin to the FeTFET with a notable distinction in the source and drain region doping.

large coercive field ensures a large voltage window between the two states. Also, La:HfO_2 has the lowest $\mathcal{E}_r$ among the other counterparts which are responsible for the highest voltage drop at the ferroelectric layer that adds to the memory window of the device. Previous research has shown that MW increases with remenant polarization of the ferroelectric material [45]. The depolarization field and gate leakage currents cause the practical MW to be less than the theoretical maximum of $2E_c \times t$ (t = thickness of ferroelectric layer). Electrons get injected into the ferroelectric layer from the gate and semiconductor, leading to charge compensation and reduced polarization [46]. Table 3 lists the theoretical maximum MW that can be achieved from the particular material at ferroelectric layer thickness of 10 nm vs. the MW obtained in this work. Due to lattice mismatch, defects, and leakage current, a buffer layer must have the right interfacing with the substrate. The ambipolar behavior is not shown here as the focus of this work is to show the MW, which remains unaffected by the ambipolarity. The term "Right interface" means that the Si:HfO_2 has a proper interface with silicon. Due to this, direct deposition of Si-doped HfO_2 thin films on the silicon substrate is possible, and this will help to reduce the leakage current.

Fig. 9 (b) presents the dependence of the MW and ON current on the ferroelectric layer material. The FeTFET implemented using PZT/SBT as ferroelectric gate material achieves higher ON current since they have higher relative permittivity than La:HfO_2 or Si:HfO_2. The tunneling current of the device is directly proportional to the surface potential. The FeTFET with La:HfO_2 ferroelectric layer experiences a very high potential drop across the ferroelectric layer due to its low dielectric constant thus, the device has the least effective surface potential. SBT/PZT FeTFET has the least potential drop because of the very high dielectric constant, thus offering the highest ON current. Table 4 compares the proposed device's electrical characteristics with previously reported research work. Over the past few years, enormous attention has been paid to the $HfZrO_x$ ferroelectric material and researchers have observed high value of the polarization and endurance for $HfZrO_x$ [49–52]. Since this study focuses on the MW of the device, thus MW and SS corresponding to the ferroelectric thickness are presented.

To examine the influence of the buffer layer on the MW, three different materials - SiO_2, Si_3N_4 and HfO_2 - each with a 1 nm thickness are investigated. The permittivity of SiO_2, Si_3N_4 and HfO_2 is 3.9, 7.5 and 16.64, respectively. As seen from Fig. 10, the MW is reduced when lower permittivity material is used. MW obtained in the case of SiO_2, Si_3N_4 and HfO_2 as buffer layers is 0.48 V, 0.76 V and 1.32 V, respectively. The highest MW is achieved in the case of HfO_2 and the lowest in the case of SiO_2. These results are justified by the fact that low permittivity materials cause a higher potential drop on the buffer layer reducing the ferroelectric voltage since the system becomes equivalent to two serial capacitors. Higher permittivity material such as HfO_2 reduces the voltage drop as well as the depolarization. Minor polarization hysteresis loops are formed rather than the desired saturation polarization loop when ferroelectric voltage is reduced. It reduces the MW significantly. It can also be seen from Fig. 10 that as we move from lower dielectric constant material (SiO_2) to higher dielectric constant material (HfO_2), the ON current increases significantly. This can be justified by the fact that higher dielectric constant increases the gate coupling with the channel, which leads to an increase in current. An increment of almost 10 times is observed as seen from Fig. 10 (b).

Fig. 11 presents the MW comparison of proposed FeTFET and FeMOSFET having the same dimensions and doping concentrations. FeMOSFETs are currently being explored in the digital and analog circuit applications and architectures [56] thus, comparing them with the proposed device is crucial. For simulating the FeFET, the source is doped with arsenic, the channel is made intrinsic while the doping concentration levels of FeMOSFET are kept the same as that of the FeTFET. The physics of the TCAD simulation model was modified to simulate the FeMOSFET structure by including models of classical physics in place of quantum physics of Band-to-Band tunneling. As seen from Fig. 11, the MW is 1.32 V and OFF current is approximately 10^{-18} A/μm in case of the proposed FeTFET whereas, the MW is 0.91 V and OFF current is approximately 10^{-15} A/μm in case of FeMOSFET. The proposed FeTFET provides larger MW and lower OFF current, thus better data retention and low static power dissipation. However, the ON current of FeTFET is low compared to the FeMOSFET, thus FeTFET lags FeMOSFET in terms of current driving capabilities. Also, the SS of the FeTFET is 28 mV/dec. which is slightly better than FeMOSFET (36 mV/dec.). Table 5 summarizes the MW achieved in the proposed device and its different variants having the same dimensions. Table 6 illustrates the evaluation of the TFET, FeTFET, and FeFET with regards to their electrical performance and manufacturing process.

5. Conclusion

To cater to ultra low-power non-volatile memory devices at highly scaled dimensions, La:HfO_2 gate stack based ferroelectric TFET is proposed in this work. Rigorous simulation work is carried out demonstrate that the proposed FeTFET utilizing La:HfO_2 outperforms the other commonly employed ferroelectric materials like PZT, SBT and Si:HfO_2 by achieving the largest MW. This improvement in MW is attributed to greater polarization and coercive field of La:HfO_2 ferroelectric material even at 10 nm thin film thickness. La:HfO_2 can be easily grown by the ALD techniques with excellent conformality, which means they are fully compatible with the 3D structure fabrication of CMOS devices. Further, FeTFET has the edge over its counterpart FeFET since TFETs have the inherent property of low OFF current and SS. Consequently, the proposed La:HfO_2 based FeTFET exhibits potential for utilization in forthcoming low-power non-volatile memory devices.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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