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Device Simulation Based Machine Learning Technique for III V TFET

Saravanan M
Department of ECE
Sri Eshwar College of Engineering
Coimbatore, India
saranecedgl@gmail.com

Eswaran Parthasarathy
Department of ECE
SRM Institute of Science and Technology, Kattankulathur,
Chennai, India
eswaranp@srmist.edu.in

Ajayan J
Department of ECE
SR University, Warangal,
Telangana, India
email2ajayan@gmail.com

Shiromani Balmukund Rahi
University School of Information and Communication Technology
Gautam Buddha University
Greater Noida, Uttar Pradesh
sbrahi@gmail.com

Abstract—Semiconductor devices are becoming increasingly sensitive to even the smallest disruptions resulting from ongoing technological advancements. The minute variations in the nanodevices have become even more discernible as they have been greatly enlarged. Before forward device scaling, it is imperative to resolve these variations thoroughly. TFETs exhibit several drawbacks, including a low on-current that hampers the operational speed, a lifespan of over a decade, ambipolar current behavior, and reduced radio frequency performance. TFETs are very promising solid-state switches for ultralow-power integrated circuits, as they effectively address the issue of power dissipation. The primary obstacles that impede the utilization of TFETs in commercial goods are the requirement for high-quality III-V materials and their derivatives with small physical dimensions, as well as limitations in layout density. This study presents a methodical approach to creating ideal Artificial Neural Network (ANN) models. This involves a thorough consideration of the influence of the ANN size on both model correctness and SPICE simulation. To provide visual representations that are appropriate for circuit simulations, the effectiveness of computer-aided design (CAD) models for innovation is assessed using powerful full-quantum modeling tools to produce visuals.

Keywords—InAs, GaSb, TFET, TCAD, III-V material, ANN, Ultra-Low power

I. INTRODUCTION

Complementary metal oxide semiconductors (CMOS) remain a reliable and widely adopted technology but face challenges with scaling and power consumption. FinFETs offer improved performance and efficiency compared to CMOS but introduce complexity and higher costs. Tunnel Field-Effect Transistors (TFETs) represent a promising avenue in semiconductor technology, owing to their potential for low-power operation and reduced leakage currents compared to conventional CMOS transistors. Significant advancements in device design, material research, and fabrication techniques have marked the evolution of TFET technology. TFETs originate from utilizing quantum tunneling for transistor operations [1]–[3]. Early research focused on theoretical models and experimental demonstrations of the TFET behavior. Initial TFET designs faced challenges related to suboptimal performance, limited scalability, and manufacturing complexities. Researchers have explored a wide range of semiconductor materials to optimize TFET performance. III-V compound semiconductors such as InAs, InGaAs, GaSb, and InSb have emerged as promising candidates because of their favorable band structures for tunneling. Novel TFET architectures have been proposed and developed to enhance device performance. These include heterostructure TFETs, vertical TFETs, and nanowire TFETs, which offer improved control over tunneling phenomena and reduced leakage currents. Advances in gate-stack engineering have enabled better electrostatic control and reduced tunneling barriers in TFETs [4]-[6].

High-k dielectric and metal gate technologies have been integrated to improve gate control and enhance device reliability. The integration of TFETs into the existing semiconductor manufacturing processes has been a significant focus of research and development. Process technologies compatible with mainstream CMOS fabrication have been explored to seamlessly integrate TFETs with existing circuitry [7]. Currently, TFET technology is still in the research and development phase, with ongoing efforts aimed at addressing key challenges, such as improving device performance, enhancing scalability, and optimizing manufacturing processes [8]-[10]. TFETs have demonstrated promising characteristics for ultralow-power applications and energy-efficient computing, making them attractive candidates for future semiconductor technologies.

Machine learning techniques have been utilized for fault detection and diagnosis in TFET devices. By analyzing device characteristics and performance data, machine-learning models can identify anomalies and predict potential failure modes, enabling proactive maintenance and reliability improvement. Explore machine-learning techniques for integrating TFETs with other semiconductor devices and materials. By analyzing the compatibility and interface properties, machine learning models can help identify optimal integration strategies and design guidelines for heterogeneous device integration. Applying machine learning techniques to TFETs offers a wide range of opportunities for device optimization, performance prediction, fault detection, design exploration, and system-level integration [11]–[12]. Machine learning can expedite the development and application of

TFET-based technologies across various domains, including electronics, computers, and other industries.

II. DEVICE STRUCTURE

The GaSb-InAs vertical TFET features a GaSb pocket and a split drain structure, as depicted in Figure 1. Indium arsenide (InAs) was used as the drain and channel, whereas gallium antimonide (GaSb) was the source material. Both dual-gate and double-gate materials were used. The channel conductivity was modulated by the GaSb pocket layer.

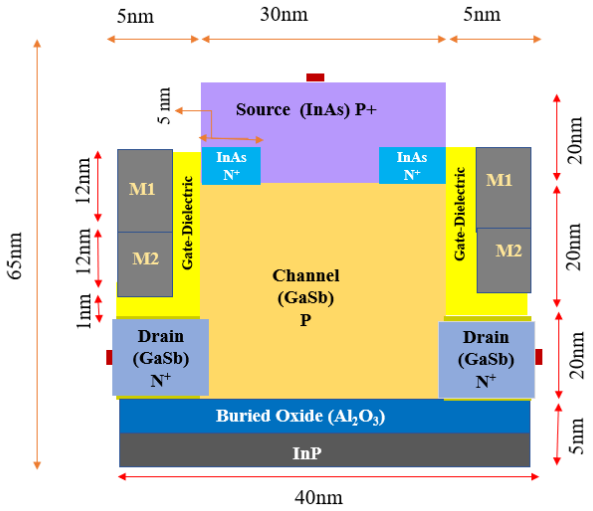

Fig.1 GaSb-InAs Vertical TFET

TABLE I: INAS-GASB VTFET DEVICE PARAMETERS

Parameters	Value
Source doping	1×10-20 cm-3
Drain doping	5×10-18 cm-3
Channel doping	1×10-16 cm-3
Channel thickness	12 nm
Gate dielectric thickness	2 nm
Channel length	30 nm
Gate work-function (M1)	4.2 eV
Gate work-function (M2)	4.6 eV

TABLE II: MATERIAL PROPERTIES USED IN THE SIMULATION

Properties	GaSb	InAs
Band-gap (eV)	0.726	0.36
Mobility of electrons (cm2/V.s)	3000	30000
Mobility of holes (cm2/V.s)	1000	240
Mass of electron m0	0.063m0	0.027m0
Mass of holes m0*	0.4m0*	0.33m0*

$$I_D \propto \exp\left[-\frac{4\sqrt{2m^*}E_g^{*\frac{3}{2}}}{3|e|\hbar\left(E_g^*+\Delta\Phi\right)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right]\Delta\Phi \qquad (1)$$

In TFETs, the drain current (I_{ON}) can exhibit characteristics that are different from those of traditional MOSFETs owing to the tunneling mechanism. TFETs typically operate at lower voltages and offer potential advantages in terms of lower leakage currents and better subthreshold swing than conventional MOSFETs.

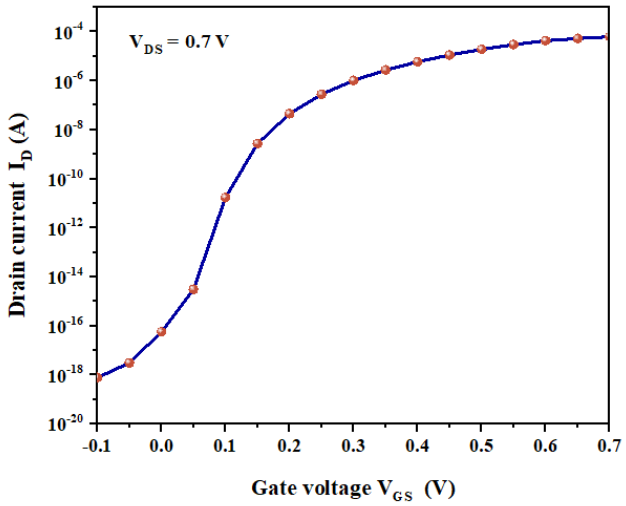

Fig.2 Transfer characteristics

The Figure-2 illustrates the I_{ON} value for this proposed model was 6.36 x 10^{-5} A/µm at V_{GS}=0.7 V and V_{DS}=0.7 V. By examining the slope of the I_{DS} vs. V_{GS} curve in the subthreshold region refer Eq (1), one can assess the TFET's ability to turn off and its potential for achieving low-power operation.

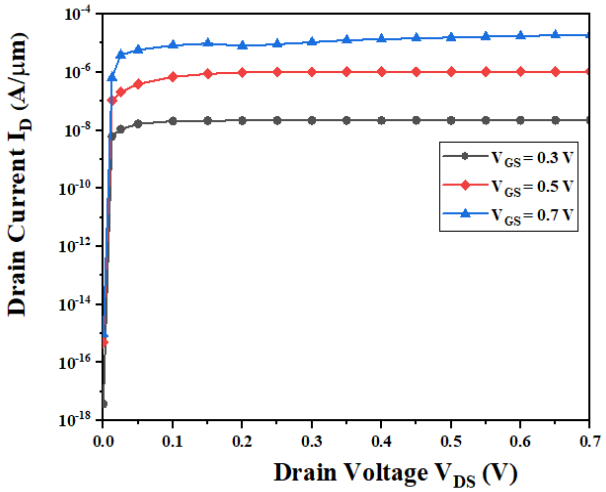

Fig.3 Output characteristics

Figure 3 shows the output characteristics of a GaSb-InAs TFET. This graph illustrates the variations in I_D and V_{DS} as functions of the V_{GS} values. In TFETs, unlike conventional MOSFETs, the drain current typically increases with decreasing drain-source voltage owing to the tunneling mechanism. This unique behavior often results in subthreshold swing values lower than the classical limit of 60 mV/decade, which is a significant advantage in low-power applications. As V_{GS} is increased beyond a certain threshold, TFETs enter the saturation region

where I_{DS} levels off. Unlike MOSFETs, TFETs do not have a distinct triode region with linear I_{DS} vs. V_{DS} behavior due to the tunneling mechanism dominating the current flow. In the subthreshold region (low V_{GS}), TFETs exhibit a nearly exponential increase in I_{DS} with increasing V_{DS} [13]. This behavior is due to the band-to-band tunneling process, which becomes more significant as the drain-source voltage increases.

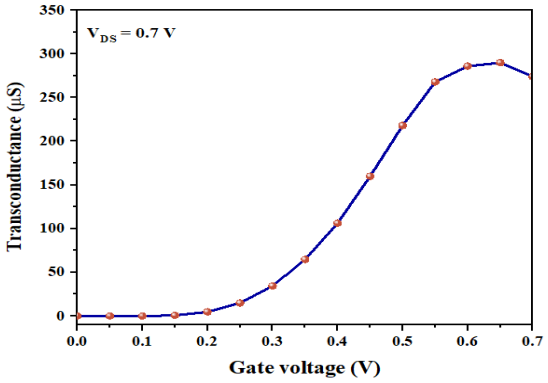

Fig.4 Transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \qquad (2)$$

In TFETs, the transconductance (g_m) is influenced by various factors, including the band-to-band tunneling mechanism, energy band structure of the semiconductor material, and device geometry. Unlike conventional MOSFETs, where transconductance is primarily determined by the carrier mobility and inversion charge, TFETs rely on the tunneling phenomenon across the bandgap. The g_m of TFETs may exhibit different characteristics compared to MOSFETs owing to the unique operating principle based on quantum tunneling. [14]

Figure 4 illustrates the g_m characteristics of the proposed device. At V_{GS}=0.7 V, V_{DS}=0.7 V g_m=274 μS/μm. The dependence of g_m on the gate bias Eq (2), device dimensions, material properties, and operating conditions makes the analysis and optimization of TFET transconductance an important aspect in TFET design and characterization. Small changes in V_{GS} can lead to significant changes in the tunneling current, affecting the transconductance. The transconductance (g_m) is related to the subthreshold slope, which quantifies the change in V_{GS} required to change the drain current by a decade. In TFETs, achieving a high-gain bandwidth product (GBP) can be challenging because of the device's unique characteristics, such as subthreshold operation and the impact of band-to-band tunneling on the small-signal behavior [15].

The GBP value was 48.9 GHZ as depicted in Figure 5. Designers often need to optimize device parameters such as gate length, gate oxide thickness, and doping profiles to achieve the desired GBP while ensuring low power consumption and acceptable levels of leakage current.

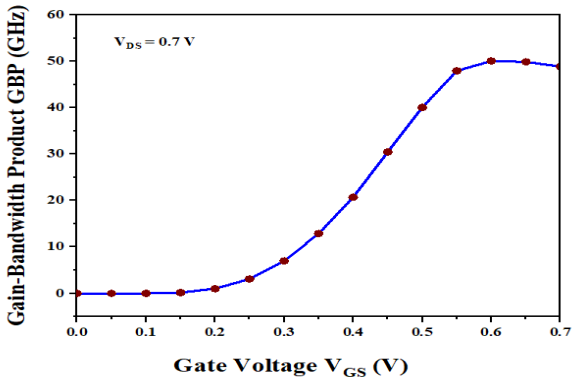

Fig.5 Gain Bandwidth Product

TABLE III INAS-GASB TFET SIMULATION RESULTS

Parameters	Values
ON Current ION (A/μm)	6.36 x 10-5
OFF Current IOFF (A/μm)	5.76 x 10-14
ION/IOFF	1.13 x 1012
Sub-threshold swing SS (mV/dec)	20.24
Threshold Voltage Vth (V)	0.25489 GHZ
Transconductance g_m (μS/μm)	274
Cut-off Frequency fT (Hz)	188 GHZ
Transit Time τ (sec)	0.59 Pico Seconds
Gain Bandwidth Product GBP (Hz)	48.9

III. MACHINE LEARNING APPROACH

Machine learning (ML) approaches in the context of TFET) involve leveraging ML algorithms and techniques to optimize the TFET design, predict device characteristics, and improve performance. A comprehensive flowchart of the machine-learning algorithm implementation is shown in Figure 6. ML algorithms can be used to develop accurate models that capture the complex behavior of TFETs. These models facilitate the simulation of device functionality under various conditions, thereby aiding the iterative design enhancement process. By identifying patterns in simulation data or real-world measurements, machine learning techniques, such as ANNs, can effectively forecast the behavior of TFETs.

Define the optimization objective, which can involve maximizing the performance metrics. such as transconductance (g_m) or minimizing metrics such as threshold voltage (Vth), leakage current, or subthreshold swing. Obtain a collection of data that encompasses the characteristics of transistors as well as the corresponding metrics of their performance. The dataset should encompass a diverse range of transistor designs, incorporating variations in the shape, material composition, doping levels, and bias settings. The data were divided into three distinct subsets: training, validation, and testing [15]. The training set imparts fresh knowledge to the ANN model, which evaluates the model parameters and prevents overfitting, and the testing set assesses the performance of the model.

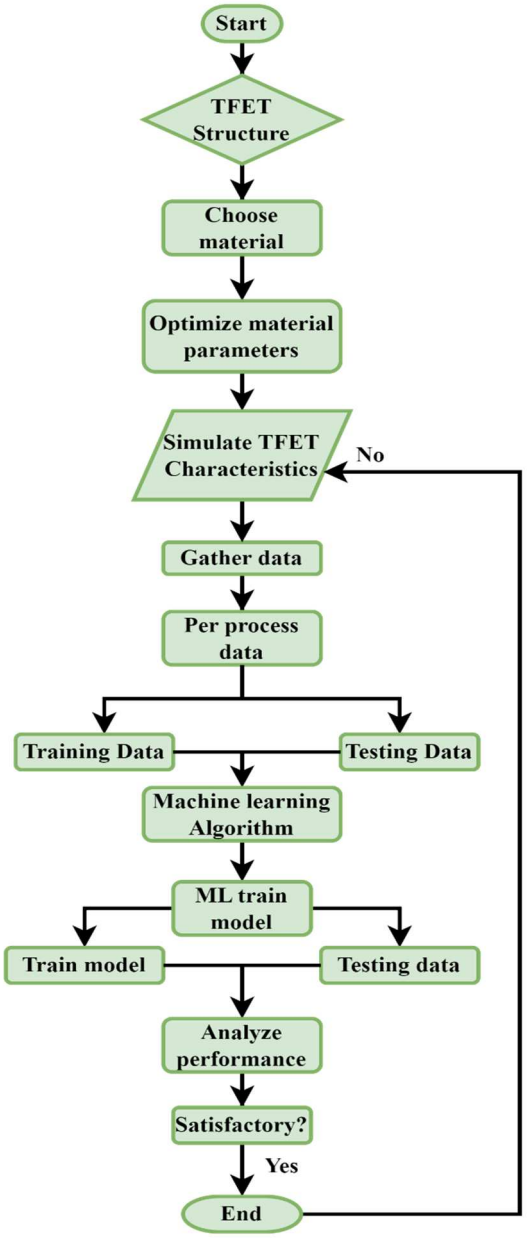

Fig.6 A comprehensive flow chart for machine learning algorithm

Develop the architecture of an artificial neural network (ANN) model to enable optimization of transistor parameters [16]. The number of layers, neurons per layer, activation functions, and regularization techniques are chosen based on the complexity of the transistor behavior and dataset characteristics. To train the ANN model, appropriate optimization techniques are used, such as Adam optimization, stochastic gradient descent (SGD), or gradient descent [13].

The validation set was used to monitor the training process and adjust the hyperparameters as required to prevent overfitting. Appropriate evaluation metrics, such as the mean squared error (MSE) or root mean squared error (RMSE), were used to assess the performance of the trained artificial neural network (ANN) model on the testing dataset. Once the ANN model was trained and validated, it was used to optimize the transistor parameters. Provide initial transistor configurations as input to the model and let it predict the optimal parameter values that maximize performance metrics or minimize undesirable characteristics [17]-[18].

The conditions that contained the real interfacial layers were accomplished by altering the prior method of manipulating the valence band offset values and using the potential gradient profit. Using thermo-voltage measurements of GaSb-InAs core-shell nanowires, scientists can accurately determine the dominant carrier type at ambient temperature and in the quantum transport domain. The quantum transport regime, even in the circumstances, because conductance measurement prohibits such a distinction from being established. In addition, people demonstrate that theoretical modeling, which uses conductance data as input, can duplicate the reported thermal voltage because it is assumed that the energy of the electron and hole states shifts differentially depending on the gate voltage applied.

$$rmse = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(Simulated\ i - Predicted\ i)^2} \quad (3)$$

It assesses the proximity between the expected and actual values Eq (3). The root mean square error (RMSE) is widely recognized as the predominant loss function in regression analysis.

$$Error\ Rate = \frac{\sigma_{Sim-}\sigma_{Pred}}{\sigma_{Sim}} X\ 100 \quad (4)$$

where σ_{Sim} and σ_{Pred} represent the standard deviation of the simulated and the ANN predicted test dataset, respectively Eq (4). SPICE is utilized for the simulation of circuits using the ANN models specifically designed for n-type and p-type TFETs. To demonstrate the application of the ANN model in circuit modeling, we replicate the inverter.

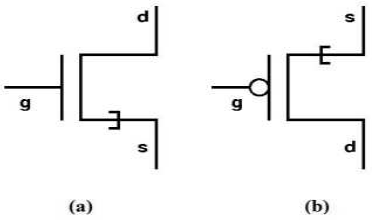

Fig. 7 Symbol of (a) nTFET and (b) pTFET

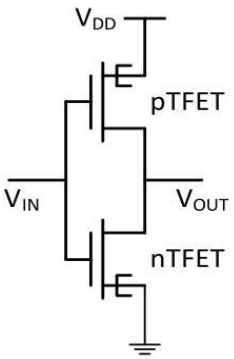

Fig. 8 TFET Inverter

Fig. 7 illustrates the n-type and p-type symbol and the TFET inverter is depicted in Figure 8.

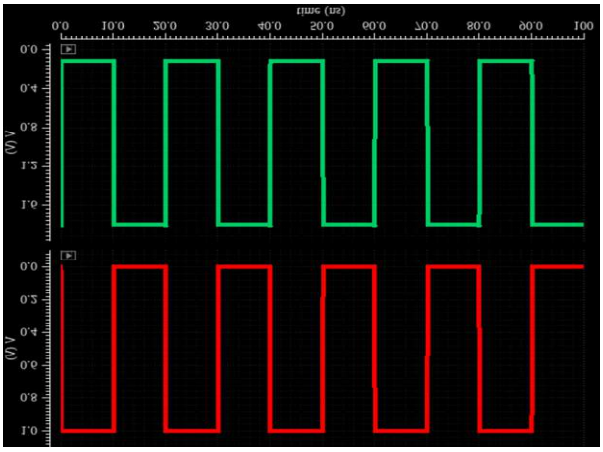

Fig. 9 TFET Inverter Output Waveform

The output waveform of the TFET inverter is shown in Figure 10. Obtain a deeper understanding of the variables that affect the performance of an ANN model and investigate methods to improve its precision and dependability [19].

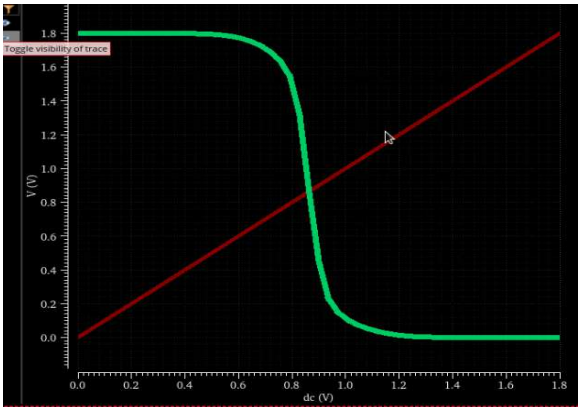

Fig. 10 Voltage Transfer Characteristics (VTC)

The training process of the ANN model was refined using input obtained from cadence simulations and experimental data. The model's structure, optimization strategies, and input features are refined to enhance its performance and capacity to generalize and assess the proximity between the expected and actual values. The root mean square error (RMSE) is widely recognized as the predominant loss function in regression analysis. The voltage-transfer characteristics of the inverter are shown in Figure 10. The input voltage (Vin) was adjusted within the range of 0V to 5V. The ANN model accurately identified change sites with a high level of dependability.

IV. CONCLUSION

This study examined the efficacy of TFETs as viable elements for constructing energy-efficient hardware platforms specifically designed for machine learning applications. TFETs exhibit favorable attributes, including sharp subthreshold slopes, less leakage currents, and decreased power consumption, in contrast to standard CMOS technology. TFETs have properties that make them very suitable for energy-efficient computation, especially when used in neural network implementations. The Voltage transfer and output characteristics of the TFET Inverter show significant concurrence with the ANN models due to their distinctive pre- and post-processing procedures. The ANN model was created using Verilog-A to accurately simulate the behavior of the circuit. The ANN models of the inverter demonstrate the same voltage transfer properties and output patterns as the ANN models. Moreover, the incorporation of TFETs into ANNs has demonstrated promising advantages in terms of diminishing power consumption and improving computing efficiency. TFETs include distinct attributes that facilitate the creation of low-power ANN structures, which are essential for applications utilized in situations with limited resources or embedded systems.

REFERENCES

{1J Ajayan, D. Nirmal, Dheena Kurian, P. Mohankumar, L. Arivazhagan, A. S. Augustine Fletcher, T. D. Subash, and M.Saravanan, “Investigation of impact of gate underlap/overlap on the analog/RF performance of composite channel double gate MOSFETs” Journal of Vacuum Science & Technology, B 37, 062201, 2019

[2] M.Saravanan, Eswaran Parthasarathy, “ A Review of III-V Tunnel Field Effect Transistors for Future Ultra Low Power Digital/Analog Applications” Microelectronics Journal, 114, 105102, 2021

[3] J. Ajayan1, D. Nirmal, P. Mohankumar, L. Arivazhagan, M.Saravanan, “LG=20 nm High Performance GaAs Substrate Based Metamorphic MOSHEMT for Next Generation High Speed Low Power Applications” Journal of Nanoelectronics and Optoelectronics, Vol. 14, pp. 1–10, 2019

[4] Mohanbabu, N Vinodhkumar, S Maheswari, S Baskaran, V Janakiraman, M Saravanan, P Murugapandiyan, “ E-Mode-Operated Advanced III-V Heterostructure Quantum Well Devices for Analog/RF and High-Power Switching Applications” Nanodevices for Integrated Circuit Design, John Wiley, pp 117-141, https://doi.org/10.1002/9781394186396.ch7

[5] M. Saravanan, Eswaran Parthasarathy, “Impact of Pocket Layer on Linearity and Analog/RF Performance of InAs-GaSb Vertical Tunnel Field-Effect Transistor”. Journal of Electronic Materials. Vol. 52, no.4, pp 2772-2779, 2023

[6] J. Ajayan1, D. Nirmal, P. Mohankumar, L. Arivazhagan, M.Saravanan, "LG = 20 nm High Performance GaAs Substrate Based Metamorphic MOSHEMT for Next Generation High Speed Low Power Applications" Journal of Nanoelectronics and Optoelectronics, Vol. 14, pp. 1–10, 2019

[7] M.Saravanan, Eswaran Parthasarathy, J. Ajayan and Nirmal,. Impact of Semiconductor Materials and Architecture Design on TFET Device Performance. Book: Emerging Low-Power Semiconductor Devices: Applications for Future Technology Nodes, CRC Press, pp 79-106, 2022.

[8] Saravanan M, Eswaran Parthasarathy, Ramkumar K, "Performance Analysis of InAs-GaAs Gate-all-around Tunnel Field Effect Transistors (GAA-TFET) for Analog/ RF applications", Journal of Physics: Conference Series, vol. 2335, no. 012043, 2022

[9] Ohashi, K., Fuhimastsu, M., Iwata, S. Miyamoto, Y, "Body width dependence of subthrehold slope and on-current in GaAsSb/InGaAs double-gate vertical tunnel FETs", Jou. of Applied Phy. Vol. 54, no. 04DF10-1, 2015

[10] Saravanan M; Eswaran Parthasarathy, "Investigation of RF/Analog Performance of InAs/InGaAs Channel Based Nanowire TFETS" DOI: 10.1109/ICCISc52257.2021.9484973, July 2021

[11] Saravanan M, Eswaran Parthasarathy, "Investigation of RF/Analog performance of Lg=16nm Planner In0.80Ga0.20As TFET" DOI: 10.1109/ICECCT52121.2021.9616769, September 2021.

[12] Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling fieldeffect transistor (TFETs) with subthreshold swing (SS) less than 60 mV/Dec," IEEE Electron Device Letters, 28 (8) p 743, 2007

[13] M Saravanan, K Ramkumar, Eswaran Parthasarathy, J Ajayan, S Sreejith, "Introduction to Conventional MOSFET and Advanced Transistor TFET, Book: Advanced Ultra Low-Power Semiconductor Devices: Design and Applications, John Wiley & Sons, Inc., pp 29-49, 2023

[14] M Saravanan, K Ramkumar, Eswaran Parthasarathy, J Ajayan, "Analog/RF Performance Analysis of TFET Device, Book: Tunneling Field Effect Transistors, CRC Press, pp 125-147, 2023

[15] Rajat Butola, Yiming Li, Sekhar Reddy Kola, "A Machine Learning Approach to Modeling Intrinsic Parameter Fluctuation of Gate-All-Around Si Nanosheet MOSFETs" IEEE Access, vol. 10, pp 71356-71368, 2022

[16] H. Wei, W. Mao, H. Fang, Z. Zhang, JX. Zhang, BJ. Lan and J. Wan, "Advanced MOSFET Model Based on Artificial Neural Network" CSTIC-2020,10.1109/CSTIC49141.2020.9282457

[17] Jing Wang, Yo-Han Kim, Jisu Ryu, Changwook Jeong, Woosung Choi, and Daesin Kim, "Artificial Neural Network-Based Compact Modeling Methodology for Advanced Transistors" IEEE Transactions on Electron Devices, vol. 68, no. 3, 2021

[18] HyunJoon Jeong, SangMin Woo, JinYoung Choi, HyungMin Cho, Yohan Kim, Member, Jeong-Taek Kong, SoYoung Kim, , "Fast and Expandable ANN-Based Compact Model and Parameter Extraction for Emerging Transistors" IEEE Journal of the Electron Devices Society, Vol. 11, PP 153 – 160, 2023

[19] Abdurrahman Ozgür Polat, Mutlu Avcı, "Modifed GRNN based atomic modeling approach for nanoscale devices and TFET implementation" Materials Today Communications, vol.27, pp 102294, 2021